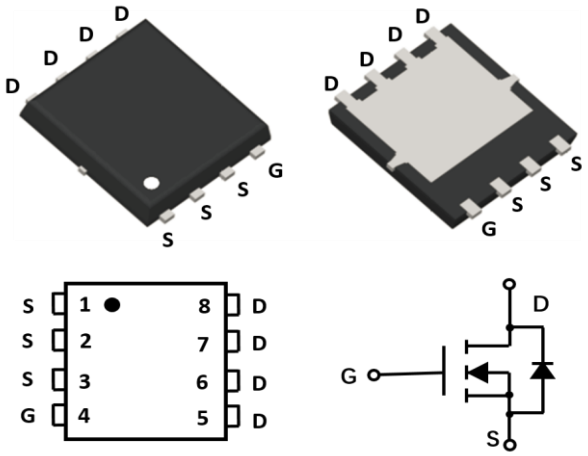
N-Channel Enhancement Mode Field Effect Transistor

PDFN5060-8L



Product Summary

- V_{DS} 40 V
- I_D 130 A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜1.8 mohm
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜3.0 mohm
- 100% UIS Tested
- 100% ▽V_{DS} Tested

General Description

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

Applications

- Consumer electronic power supply
- Motor control
- Synchronous- rectification
- Invertors

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	40	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current [A]	Tc=25℃	I_D	130	A
	Tc=100℃		82	
Pulsed Drain Current [B]		I_{DM}	390	A
Avalanche energy [C]		E_{AS}	200	mJ
Total Power Dissipation [D]	Tc=25℃	P_D	140	W
	Tc=100℃		56	
Thermal Resistance Junction-to-Case		$R_{\theta JC}$	0.89	℃/ W
Thermal resistance, junction-ambient [E]		$R_{\theta JA}$	62	
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG130G04A	F1	YJG130G04A	5000	10000	100000	13“ reel

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	40			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40V,V_{GS}=0V			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1.0	1.8	2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= 10V, I_D=55A		1.3	1.8	mΩ
		V_{GS}= 4.5V, I_D=55A		2.0	3.0	
Diode Forward Voltage	V_{SD}	I_S=20A,V_{GS}=0V			1.3	V
Maximum Body-Diode Continuous Current	I_S				130	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=20V,V_{GS}=0V,f=1MHZ		6587		pF
Output Capacitance	C_{oss}			2537		
Reverse Transfer Capacitance	C_{rss}			179		
Switching Parameters						
Total Gate Charge	$Q_{g\ (10V)}$	V_{GS}=10V,V_{DS}=20V,I_D=20A		96.8		nC
Total Gate Charge	$Q_{g\ (4.5V)}$			41.1		
Gate-Source Charge	Q_{gs}			14.5		
Gate-Drain Charge	Q_{gd}			18.4		
Reverse Recovery Chrage	Q_{rr}	I_F=20A, di/dt=100A/us		557		
Reverse Recovery Time	t_{rr}			205		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V, V_{DD}=20V, R_L=2Ω I_D=20A		26.6		
Turn-on Rise Time	t_r			9.3		
Turn-off Delay Time	$t_{D(off)}$			96		
Turn-off fall Time	t_f			39		

A. Calculated continuous current based on maximum allowable junction temperature.
B. Repetitive rating; pulse width limited by max. junction temperature.
C. V_{DD}=30 V, R_G=50 Ω, L=0.3 mH, starting T_j=25 ℃.
D. Pd is based on max. junction temperature, using junction-case thermal resistance.
E. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25 ℃.

■ Typical Performance Characteristics

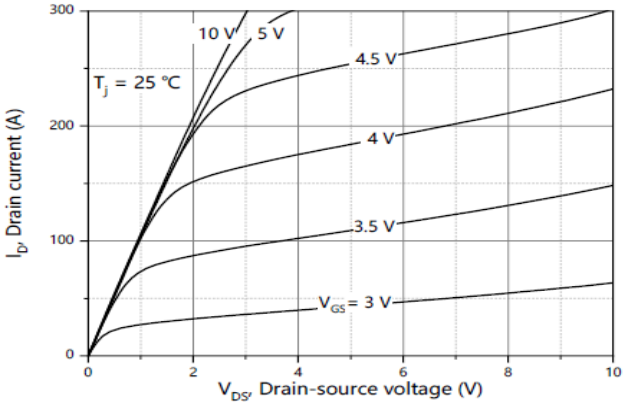


Figure1. Output Characteristics

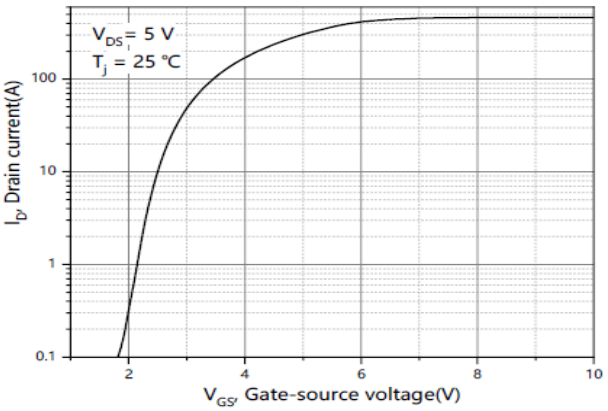


Figure2. Transfer Characteristics

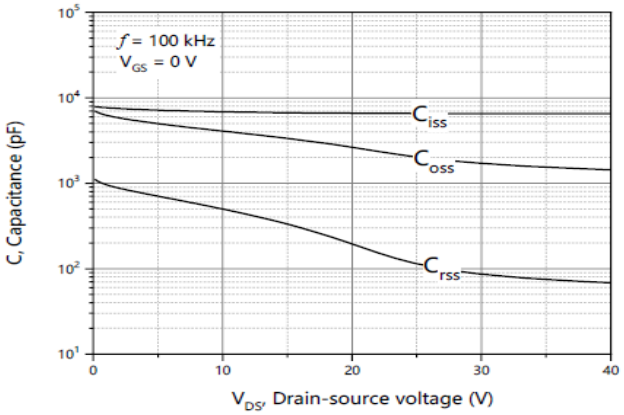


Figure3. Capacitance Characteristics

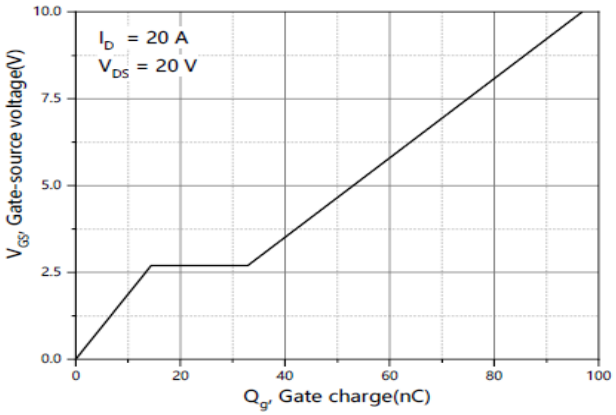


Figure4. Gate Charge

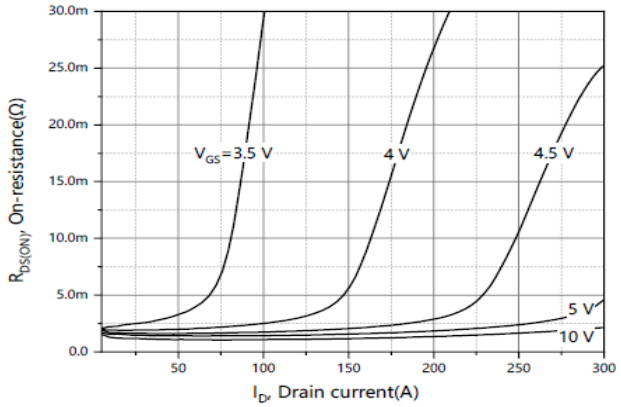


Figure5. Drain-Source on Resistance

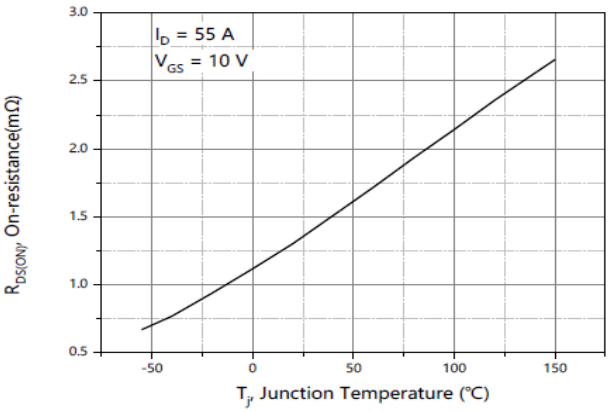


Figure6. Drain-Source on Resistance

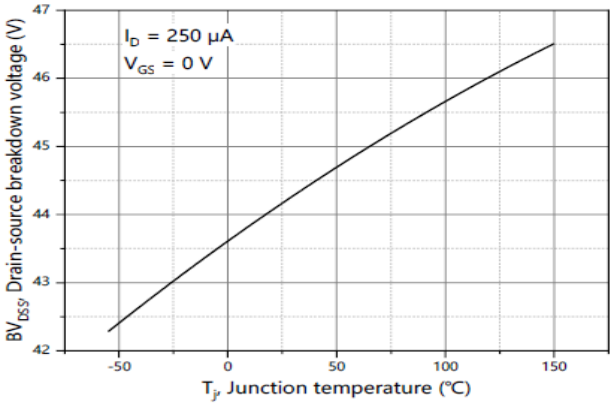


Figure7. Drain-Source Breakdown Voltage

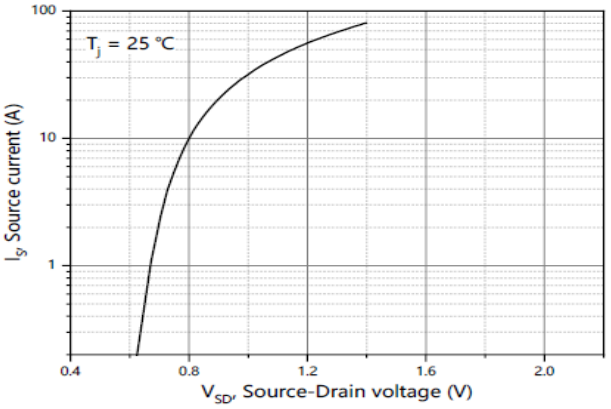


Figure8. Forward Characteristic of Body Diode

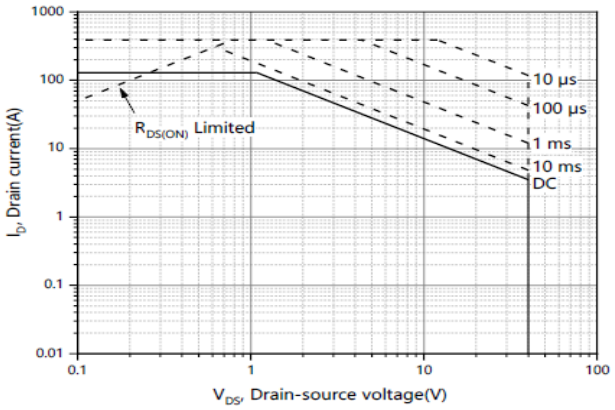


Figure9. Safe Operation Area

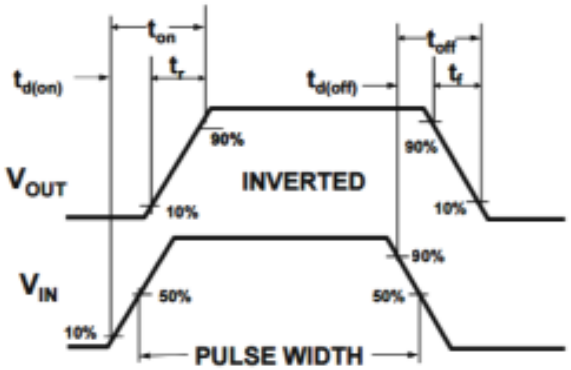
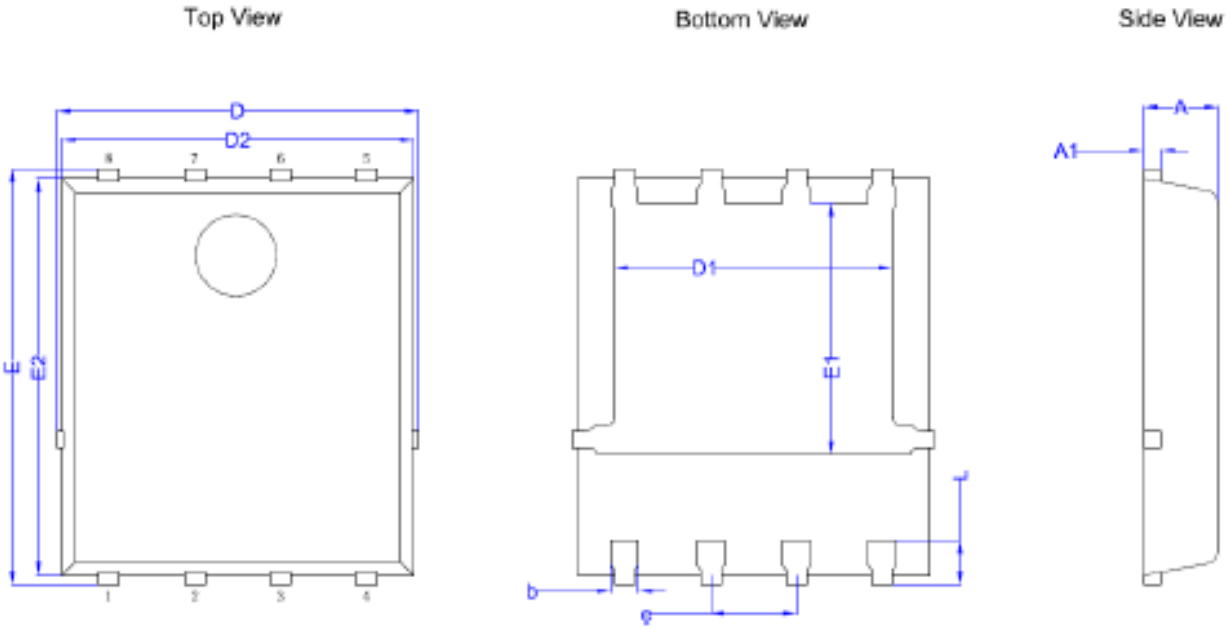


Figure10. Switching wave

■ PDFN5060-8L Package information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.00	1.10	1.20
A1		0.254 BSC	
D	5.15	5.35	5.55
E	5.95	6.15	6.35
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
e		1.27BSC	
b	0.31	0.41	0.51
L	0.56	0.66	0.76

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