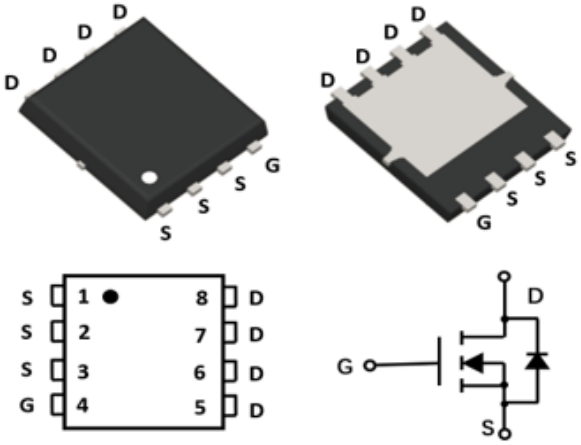
N-Channel Enhancement Mode Field Effect Transistor

PDFN 5X6



Product Summary

- V_{DS} 150V
- I_D(Silicon limited) 85A
- I_D(Package limited) 63A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜15 mohm
- 100% UIS Tested
- 100% ▽V_{DS} Tested

General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

Applications

- Synchronous Rectification
- AC-DC and DC-DC Power Supplies
- AC-DC Adapters(USB PD) SR
- Load Switch

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	150	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current (Silicon limited)		I_D	85	A
Drain Current (Package limited)	Tc=25℃	I_D	63	A
	Tc=100℃		40	
Pulsed Drain Current [A]		I_{DM}	325	A
Avalanche energy [B]		E_{AS}	290	mJ
Total Power Dissipation [C]	Tc=25℃	P_D	120	W
	Tc=100℃		48	
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

■Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient [D]	t≤10S	$R_{\theta JA}$	15	20	℃/W
Thermal Resistance Junction-to-Ambient [D]	Steady-State		40	50	
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	0.84	1.04	

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG85G15A	F1	YJG85G15A	5000	10000	100000	13“ reel

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	150			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=150V,V_{GS}=0V			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	2.5	3.5	4.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A		11	15	mΩ
Diode Forward Voltage	V_{SD}	I_S=20A,V_{GS}=0V			1.3	V
Maximum Body-Diode Continuous Current	I_S				85	A
Gate resistance	R_G	f=1MHz, Open drain		1.6		Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=75V,V_{GS}=0V,f=1MHZ		3980		pF
Output Capacitance	C_{oss}			800		
Reverse Transfer Capacitance	C_{rss}			20		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=75V,I_D=20A		53.9		nC
Gate-Source Charge	Q_{gs}			22.3		
Gate-Drain Charge	Q_{gd}			5.14		
Reverse Recovery Chrage	Q_{rr}	I_F=20A, di/dt=100A/us		320		
Reverse Recovery Time	t_{rr}			100.8		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V, V_{DD}=75V,I_D=20A R_{GEN}=3Ω		21		
Turn-on Rise Time	t_r			22.5		
Turn-off Delay Time	$t_{D(off)}$			36.2		
Turn-off fall Time	t_f			28.5		

A. Repetitive rating; pulse width limited by max. junction temperature.
B. V_{DD}=50V, R_G=25Ω, L=5mH.
C. Pd is based on max. junction temperature, using junction-case thermal resistance.
D. The value of RθJA is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with TA =25° C. The Power dissipation PDSM is based on RθJA t≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

■ Typical Performance Characteristics

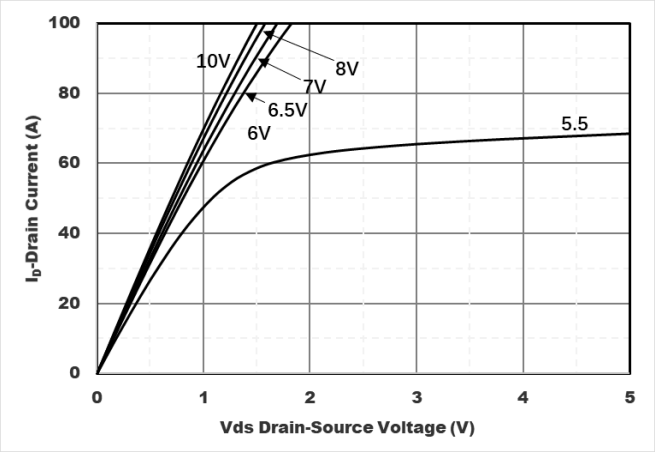


Figure1. Output Characteristics

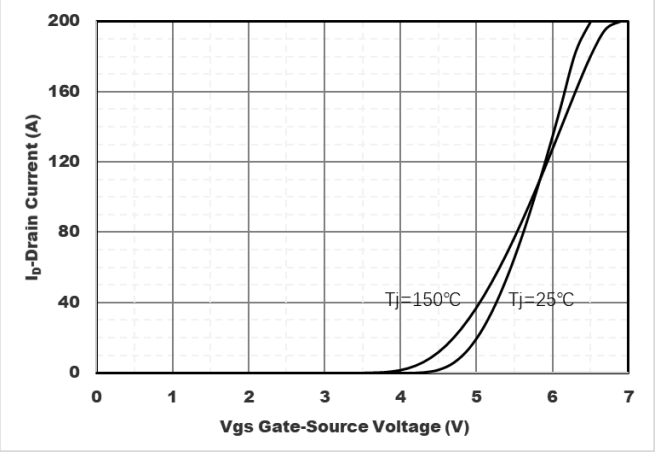


Figure2. Transfer Characteristics

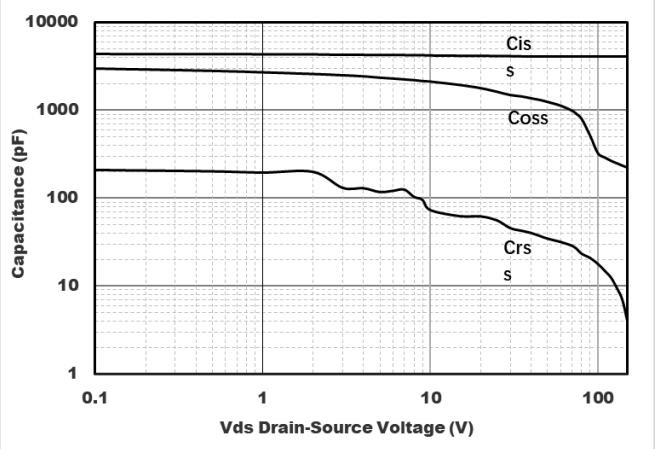


Figure3. Capacitance Characteristics

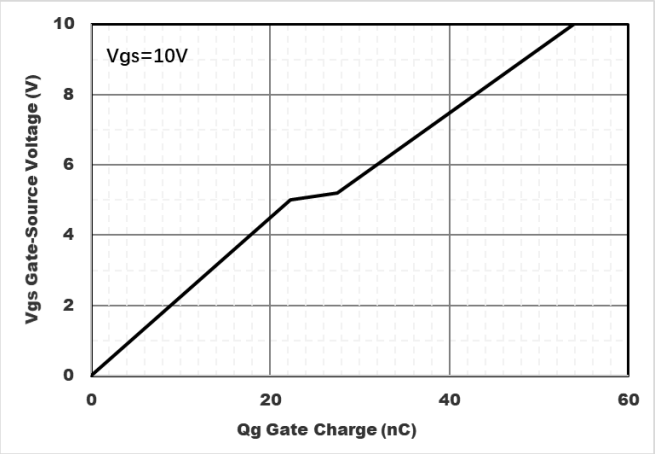


Figure4. Gate Charge

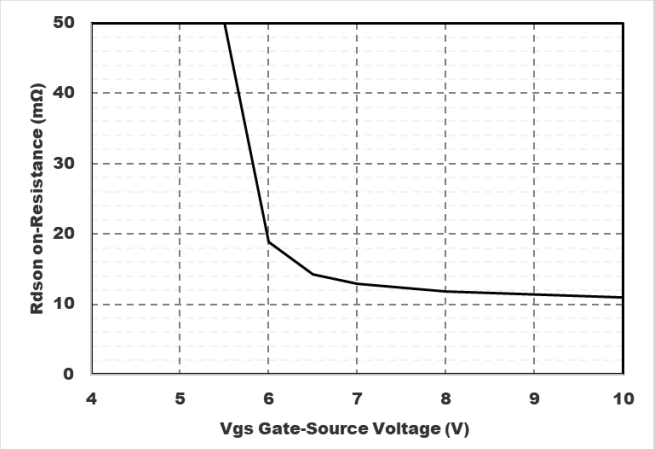


Figure5. : On-Resistance vs. Gate to Source Voltage

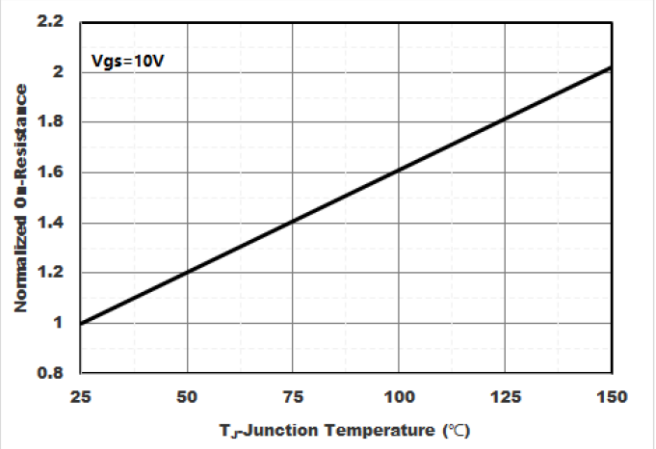


Figure6.Normalized On-Resistance

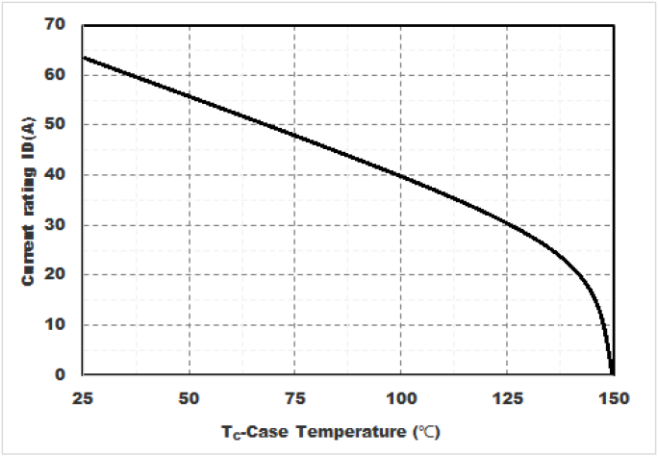


Figure7. Drain current

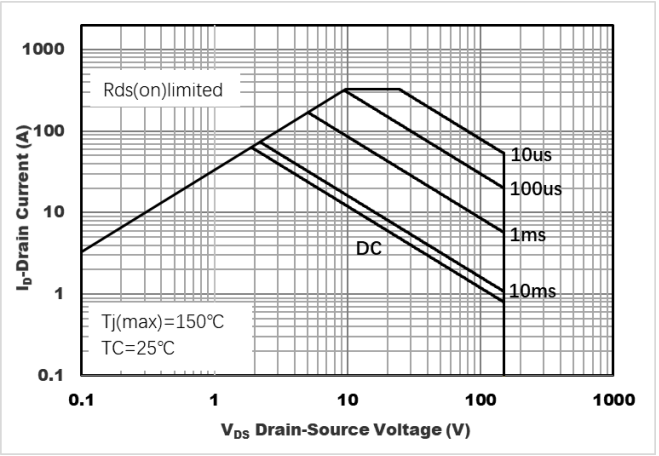


Figure8.Safe Operation Area

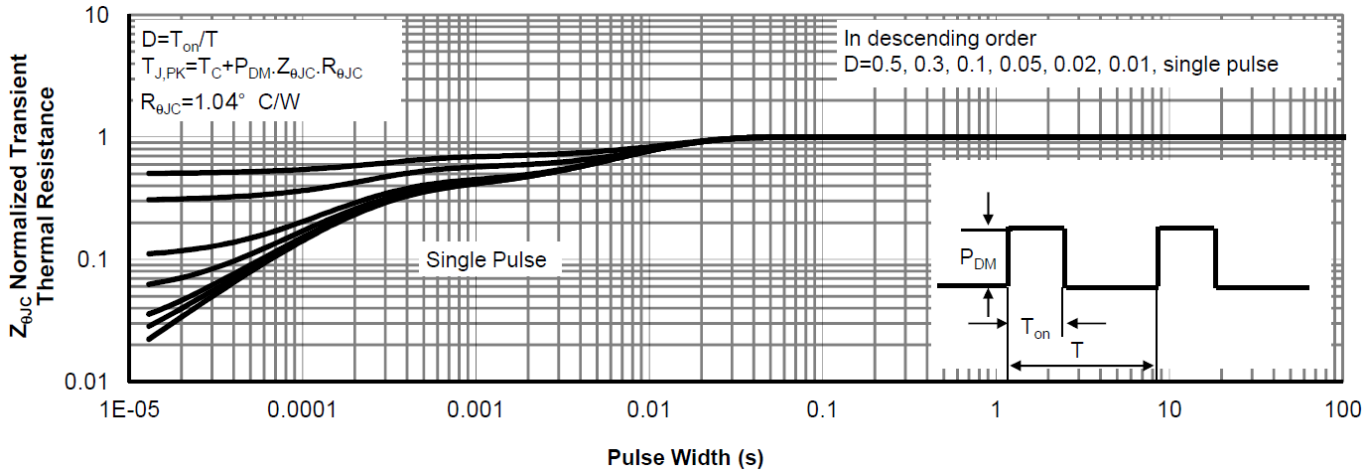
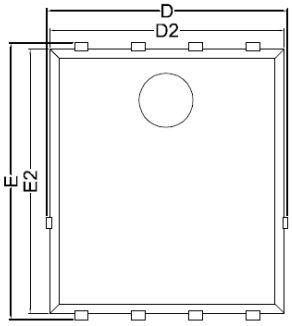
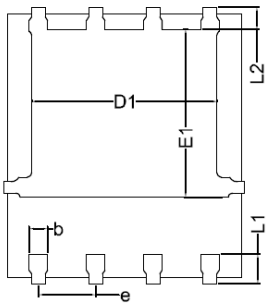


Figure9.Normalized Maximum Transient thermal impedance

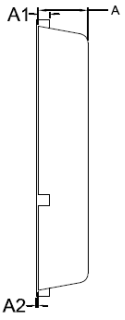
■ PDFN5x6 Package Information



Top View
正面视图



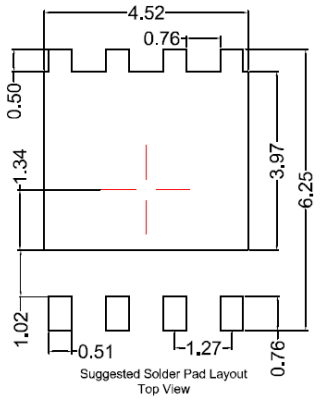
Bottom View
背面视图



Side View
侧面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1		0.254 BSC	
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
L1	0.56	0.66	0.76
L2		0.50 BSC	
b	0.31	0.41	0.51
e		1.27 BSC	

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.



Suggested Solder Pad Layout
Top View

Disclaimer

The information presented in this document is for reference only. Yangzhou Yangjie Electronic Technology Co., Ltd. reserves the right to make changes without notice for the specification of the products displayed herein to improve reliability, function or design or otherwise.

The product listed herein is designed to be used with ordinary electronic equipment or devices, and not designed to be used with equipment or devices which require high level of reliability and the malfunction of with would directly endanger human life (such as medical instruments, transportation equipment, aerospace machinery, nuclear-reactor controllers, fuel controllers and other safety devices), Yangjie or anyone on its behalf, assumes no responsibility or liability for any damages resulting from such improper use of sale.

This publication supersedes & replaces all information previously supplied. For additional information, please visit our website http:// www.21yangjie.com , or consult your nearest Yangjie's sales office for further assistance.