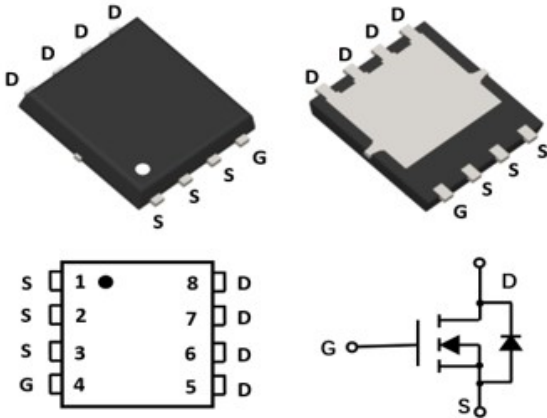


## N-Channel Enhancement Mode Field Effect Transistor

### PDFN 5X6



### Product Summary

- $V_{DS}$  60V
- $I_D$  53A
- $R_{DS(ON)}$ ( at  $V_{GS}=10V$ ) < 8.2 mohm
- $R_{DS(ON)}$ ( at  $V_{GS}=4.5V$ ) < 12 mohm
- 100% UIS Tested
- 100%  $\nabla V_{DS}$  Tested

### General Description

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$

### Applications

- DC-DC Converters
- Power management functions
- Industrial and Motor Drive application

### ■ Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	60	V
Gate-source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current	$T_c=25^\circ\text{C}$	$I_D$	53	A
	$T_c=100^\circ\text{C}$		34	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	160	A
Avalanche energy <sup>B</sup>		$E_{AS}$	195	mJ
Total Power Dissipation	$T_c=25^\circ\text{C}$	$P_D$	65	W
	$T_c=100^\circ\text{C}$		26	
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~+150	$^\circ\text{C}$

### ■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient <sup>D</sup>	$t \leq 10\text{S}$	$R_{\theta JA}$	16	20	$^\circ\text{C/W}$
Thermal Resistance Junction-to-Ambient <sup>D</sup>	Steady-State		45	55	
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	1.5	1.9	

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG53G06A	F1	YJG53G06A	5000	10000	100000	13" reel



# YJG53G06A

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =250μA	60			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V	T <sub>J</sub> =25°C		1	μA
			T <sub>J</sub> =55°C		5	
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250μA	1.2	1.7	2.5	V
Static Drain-Source On-Resistance	R <sub>Ds(ON)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> =20A		6.8	8.2	mΩ
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> =10A		9.5	12	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =20A, V <sub>GS</sub> =0V		0.8	1.2	V
Maximum Body-Diode Continuous Current	I <sub>S</sub>				53	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =35V, V <sub>GS</sub> =0V, f=1MHZ		1525		pF
Output Capacitance	C <sub>oss</sub>			372		
Reverse Transfer Capacitance	C <sub>rss</sub>			13.5		
Gate Resistance	R <sub>g</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =0V, f=1MHZ		1.6		Ω
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub> (10V)	V <sub>GS</sub> =10V, V <sub>DS</sub> =30V, I <sub>D</sub> =20A		31		nC
Total Gate Charge	Q <sub>g</sub> (4.5V)			11.3		
Gate-Source Charge	Q <sub>gs</sub>			6		
Gate-Drain Charge	Q <sub>gd</sub>			5		
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =20A, di/dt=500A/us		18		
Reverse Recovery Time	t <sub>rr</sub>			30		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =10V, V <sub>DD</sub> =30V, R <sub>L</sub> =2.5Ω R <sub>GEN</sub> =3Ω		10		ns
Turn-on Rise Time	t <sub>r</sub>			34		
Turn-off Delay Time	t <sub>D(off)</sub>			26.2		
Turn-off fall Time	t <sub>f</sub>			45		

A. Repetitive rating; pulse width limited by max. junction temperature.

B. V<sub>DD</sub>=50V, R<sub>G</sub>=25Ω, L=0.5mH, I<sub>AS</sub>=25A,.

C. Pd is based on max. junction temperature, using junction-case thermal resistance.

D. The value of R<sub>qJA</sub> is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with TA =25°C. The Power dissipation PDSM is based on R<sub>qJA</sub> t<sub>s</sub> ≤ 10s and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.



## ■ Typical Performance Characteristics

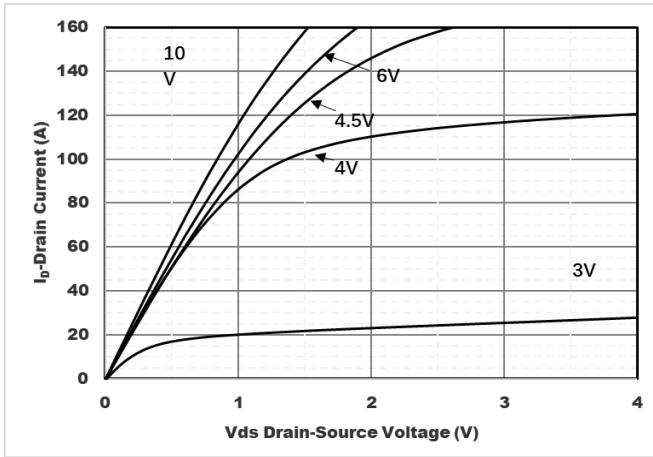


Figure1. Output Characteristics

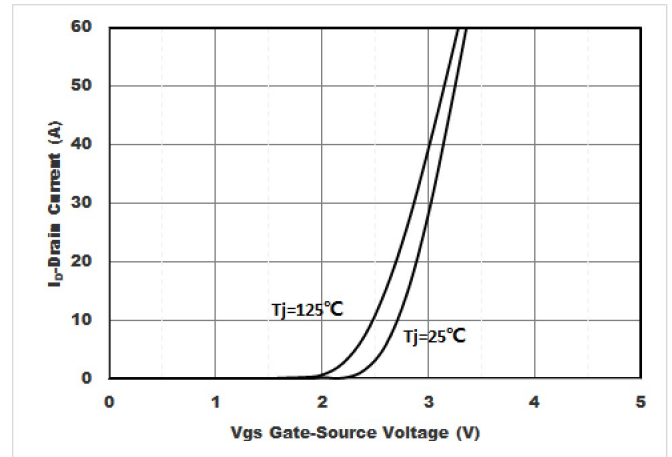


Figure2. Transfer Characteristics

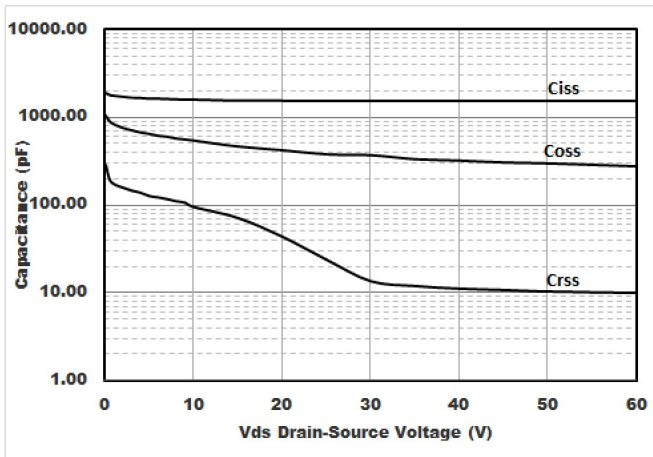


Figure3. Capacitance Characteristics

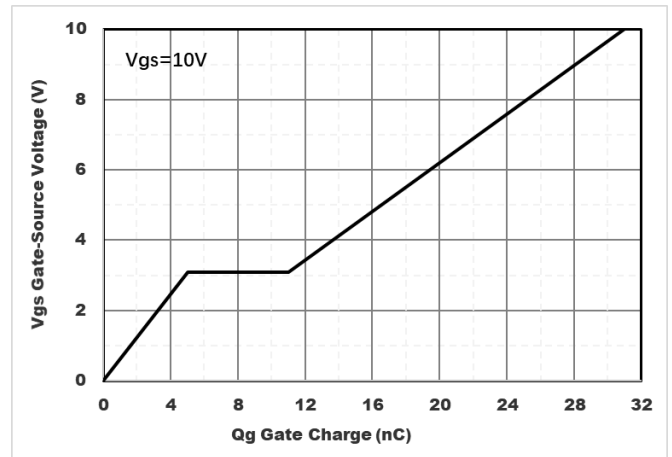


Figure4. Gate Charge

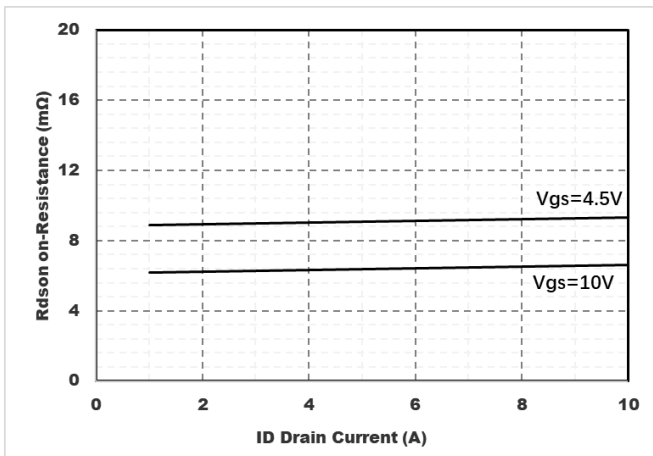


Figure5. Drain-Source on Resistance

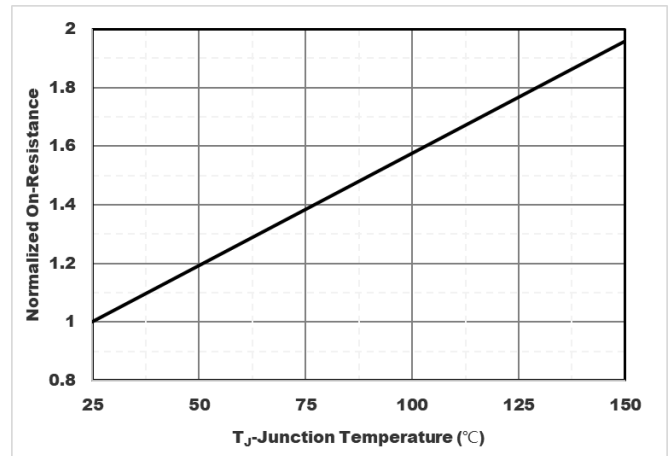


Figure6. Normalized On-Resistance



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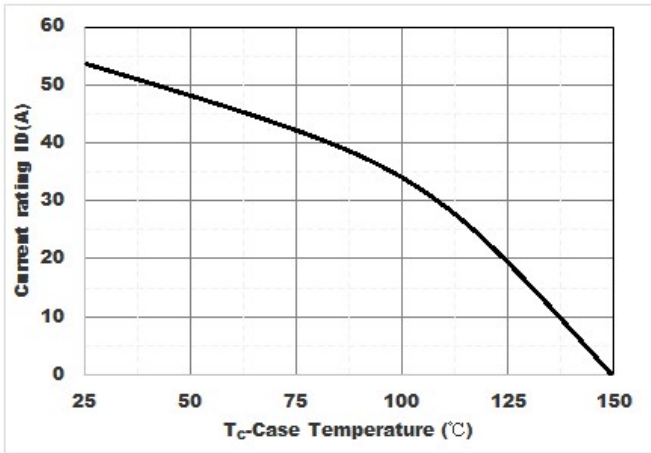


Figure7. Drain current

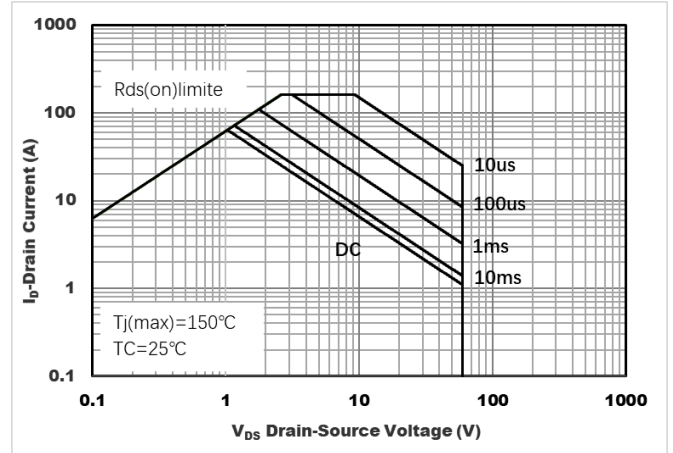


Figure8. Safe Operation Area

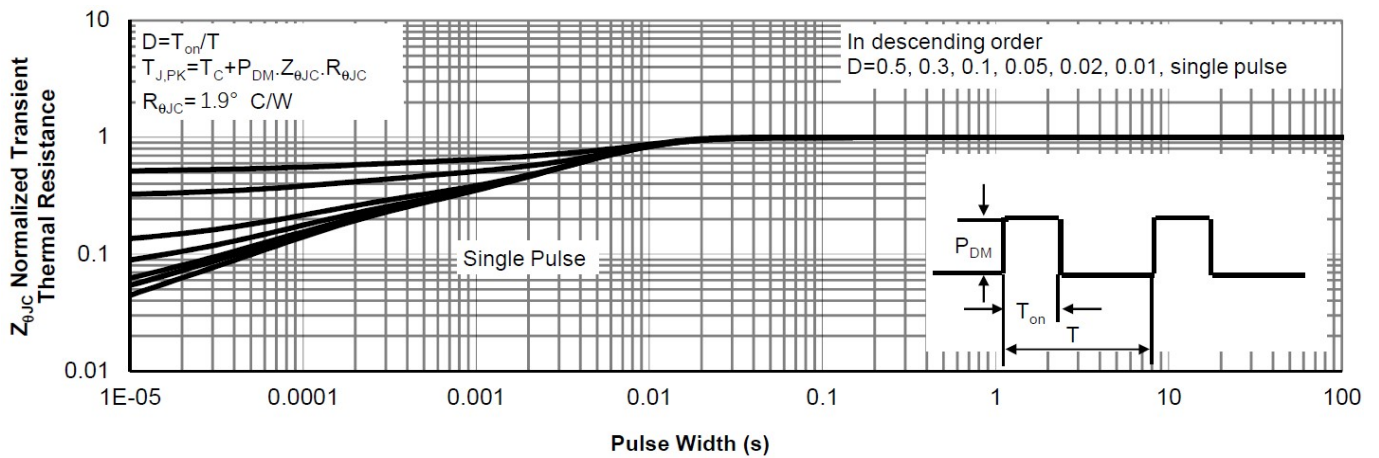
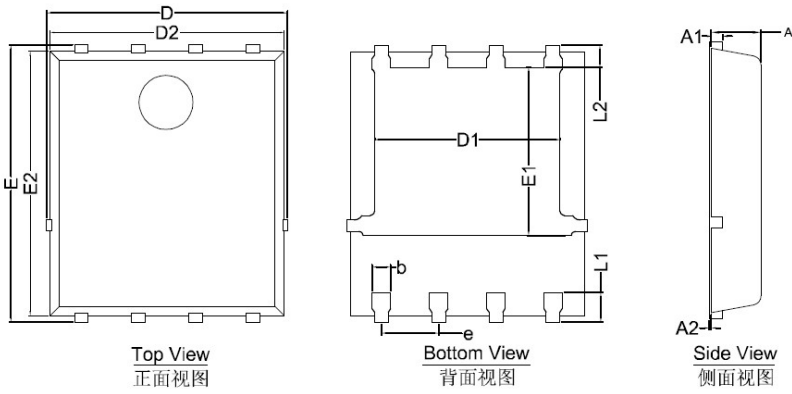


Figure9. Normalized Maximum Transient Thermal Impedance

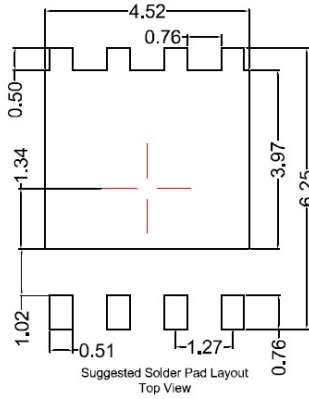


# YJG53G06A

## ■ PDFN5x6 Package information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		



Note:  
 1. Controlling dimension: in millimeters.  
 2. General tolerance:  $\pm 0.10$  mm.  
 3. The pad layout is for reference purposes only.



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