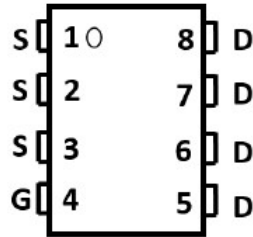
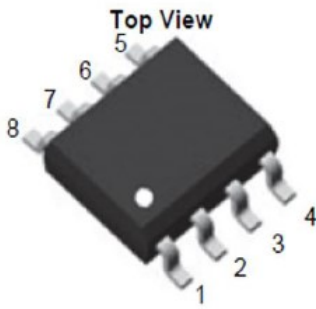
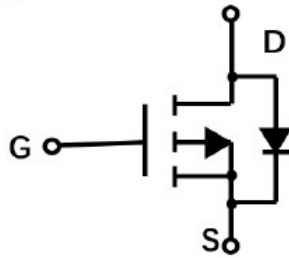


## P-Channel Enhancement Mode Field Effect Transistor



**SOP-8**



### Product Summary

- $V_{DS}$  -30V
- $I_D$  -5.1A
- $R_{DS(ON)}$  (at  $V_{GS}=-10V$ ) <43mohm
- $R_{DS(ON)}$  (at  $V_{GS}=-4.5V$ ) <59mohm
- 100%  $\nabla V_{DS}$  Tested

### General Description

- Trench Power LV MOSFET technology
- High density cell design for low  $R_{DS(ON)}$
- High Speed switching

### Applications

- Battery protection
- Load switching
- Power management

### ■ Absolute Maximum Ratings ( $T_A=25^\circ C$ unless otherwise noted)

| Parameter   | Symbol          | Limit            | Unit         |
|---|-----------------|------------------|--------------|
| Drain-source Voltage                                | $V_{DS}$        | -30              | V            |
| Gate-source Voltage                                 | $V_{GS}$        | $\pm 20$         | V            |
| Drain Current                                       | $I_D$           | $T_A=25^\circ C$ | -5.1         |
|   |                 | $T_A=70^\circ C$ | -4.1         |
| Pulsed Drain Current <sup>A</sup>                   | $I_{DM}$        | -20              | A            |
| Total Power Dissipation                             | $P_D$           | $T_A=25^\circ C$ | 2.5          |
|   |                 | $T_A=70^\circ C$ | 1.6          |
| Thermal Resistance Junction-to-Ambient <sup>B</sup> | $R_{\theta JA}$ | 50               | $^\circ C/W$ |
| Junction and Storage Temperature Range              | $T_J, T_{STG}$  | -55~+150         | $^\circ C$   |

### ■ Ordering Information (Example)

| PREFERRED P/N | PACKING CODE | Marking | MINIMUM PACKAGE(pcs) | INNER BOX QUANTITY(pcs) | OUTER CARTON QUANTITY(pcs) | DELIVERY MODE |
|---------------|--------------|---------|----------------------|-------------------------|----------------------------|---------------|
| YJS9435A      | F2           | Q9435   | 4000                 | 8000                    | 64000                      | 13" reel      |



# YJS9435A

## ■ Electrical Characteristics ( $T_J=25^\circ\text{C}$ unless otherwise noted)

| Parameter                         | Symbol       | Conditions  | Min  | Typ   | Max       | Units      |
|-----------------------------------|--------------|---|------|-------|-----------|------------|
| <b>Static Parameter</b>           |              |   |      |       |           |            |
| Drain-Source Breakdown Voltage    | $BV_{DSS}$   | $V_{GS}=0V, I_D=-250\mu A$                                | -30  |       |           | V          |
| Zero Gate Voltage Drain Current   | $I_{DSS}$    | $V_{DS}=-30V, V_{GS}=0V$                                  |      |       | -1        | $\mu A$    |
| Gate-Body Leakage Current         | $I_{GSS}$    | $V_{GS}=\pm 20V, V_{DS}=0V$                               |      |       | $\pm 100$ | nA         |
| Gate Threshold Voltage            | $V_{GS(th)}$ | $V_{DS}=V_{GS}, I_D=-250\mu A$                            | -1.0 | -1.5  | -2.4      | V          |
| Static Drain-Source On-Resistance | $R_{DS(on)}$ | $V_{GS}=-10V, I_D=-4A$                                    |      | 30    | 43        | m $\Omega$ |
|                                   |              | $V_{GS}=-4.5V, I_D=-3.5A$                                 |      | 46    | 59        |            |
| Diode Forward Voltage             | $V_{SD}$     | $I_S=-4A, V_{GS}=0V$                                      |      |       | -1.2      | V          |
| <b>Dynamic Parameters</b>         |              |   |      |       |           |            |
| Input Capacitance                 | $C_{iss}$    | $V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$                   |      | 719   |           | pF         |
| Output Capacitance                | $C_{oss}$    |   |      | 78    |           |            |
| Reverse Transfer Capacitance      | $C_{rss}$    |   |      | 64    |           |            |
| <b>Switching Parameters</b>       |              |   |      |       |           |            |
| Total Gate Charge                 | $Q_g$        | $V_{GS}=-10V, V_{DS}=-15V, I_D=-5.1A$                     |      | 14.23 |           | nC         |
| Gate-Source Charge                | $Q_{gs}$     |   |      | 3.16  |           |            |
| Gate-Drain Charge                 | $Q_{gd}$     |   |      | 2     |           |            |
| Reverse Recovery Charge           | $Q_{rr}$     | $I_F=-5.1A, di/dt=100A/\mu s$                             |      | 5.3   |           | ns         |
| Reverse Recovery Time             | $t_{rr}$     |   |      | 30    |           |            |
| Turn-on Delay Time                | $t_{D(on)}$  | $V_{GS}=-10V, V_{DS}=-15V, I_D=5.1A$<br>$R_{GEN}=3\Omega$ |      | 7.4   |           | ns         |
| Turn-on Rise Time                 | $t_r$        |   |      | 37    |           |            |
| Turn-off Delay Time               | $t_{D(off)}$ |   |      | 31.6  |           |            |
| Turn-off fall Time                | $t_f$        |   |      | 42    |           |            |

A. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty cycle  $\leq 2\%$ .

B.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design, while  $R_{\theta JA}$  is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



■ Typical Performance Characteristics

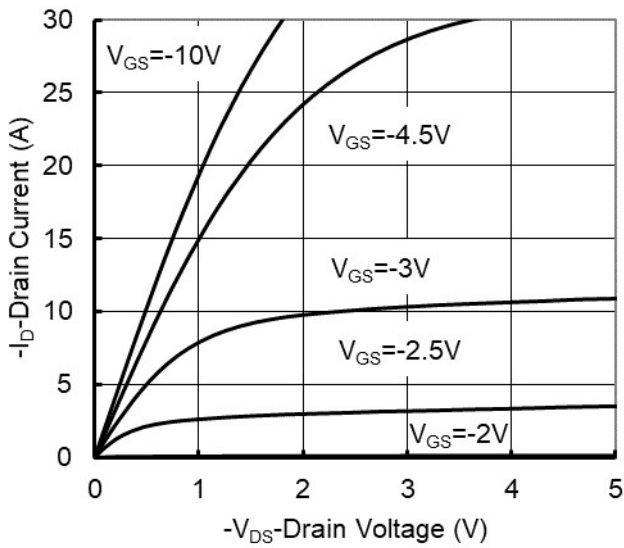


Figure1. Output Characteristics

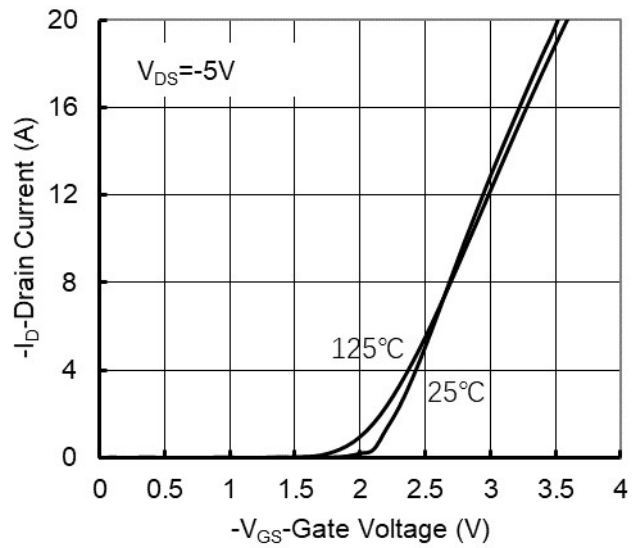


Figure2. Transfer Characteristics

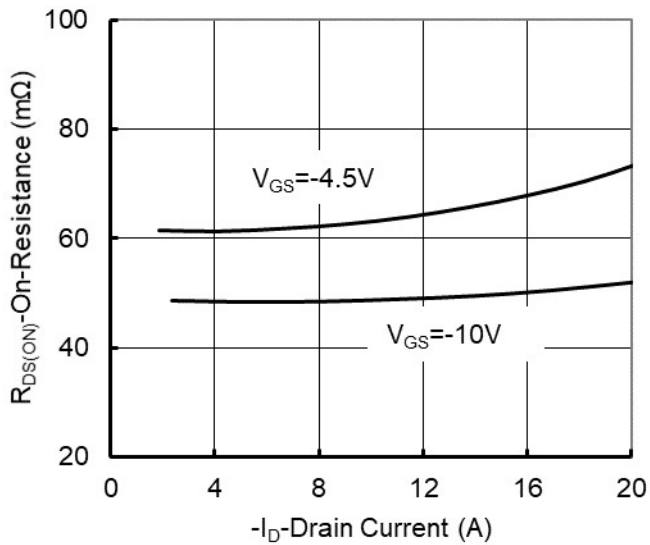


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

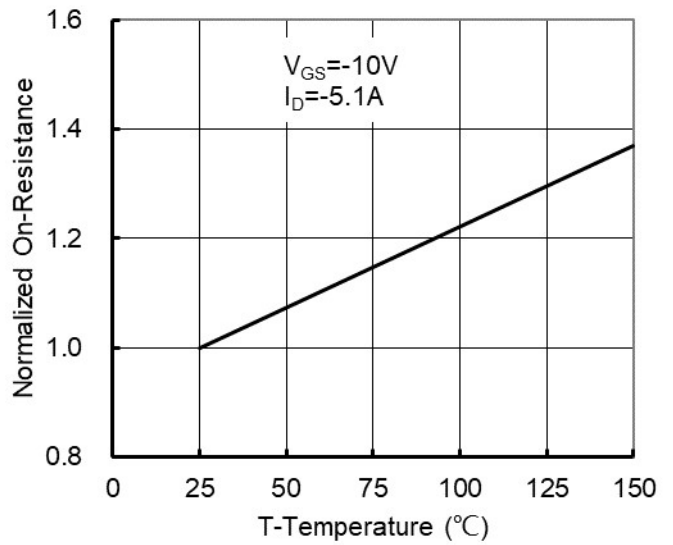


Figure 4: On-Resistance vs. Junction Temperature

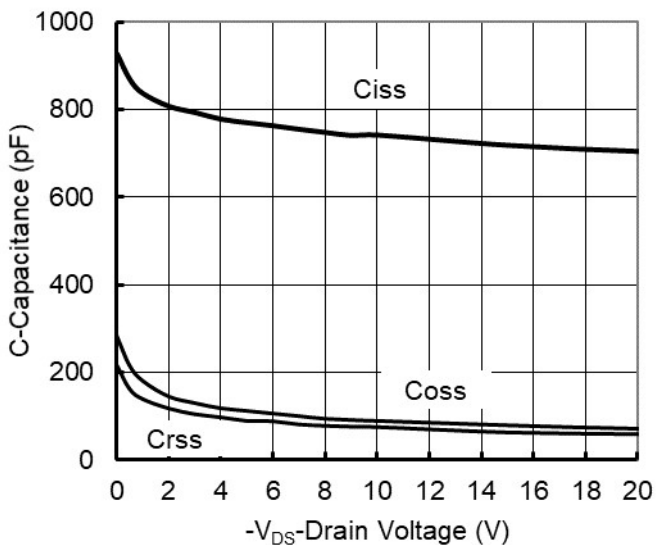


Figure5. Capacitance Characteristics

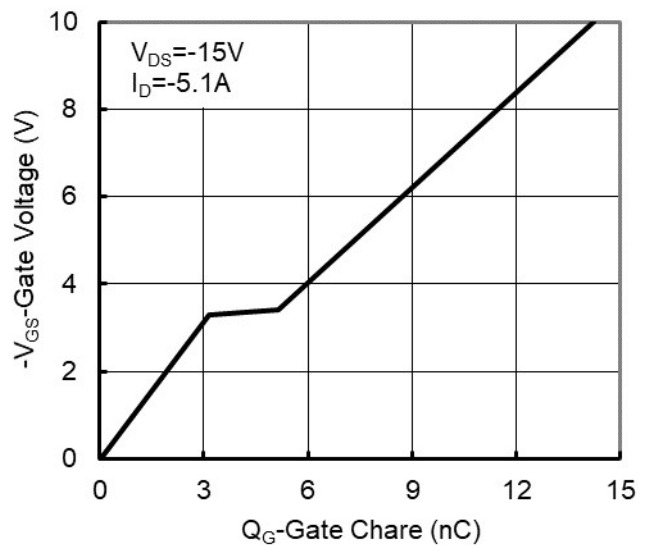


Figure6. Gate Charge

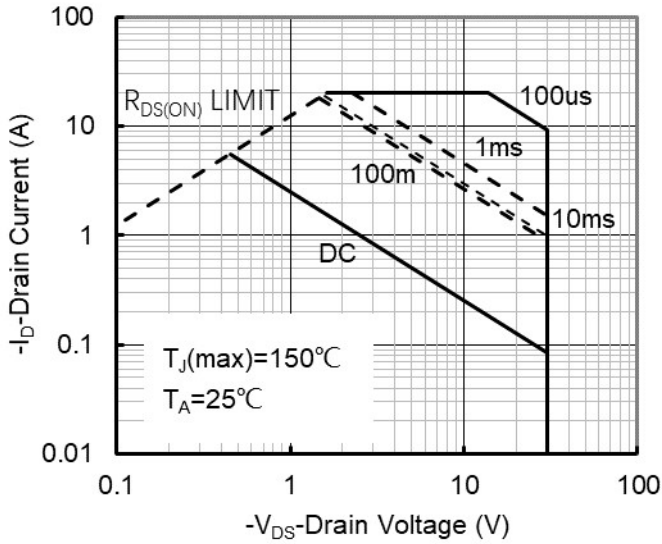


Figure7. Safe Operation Area

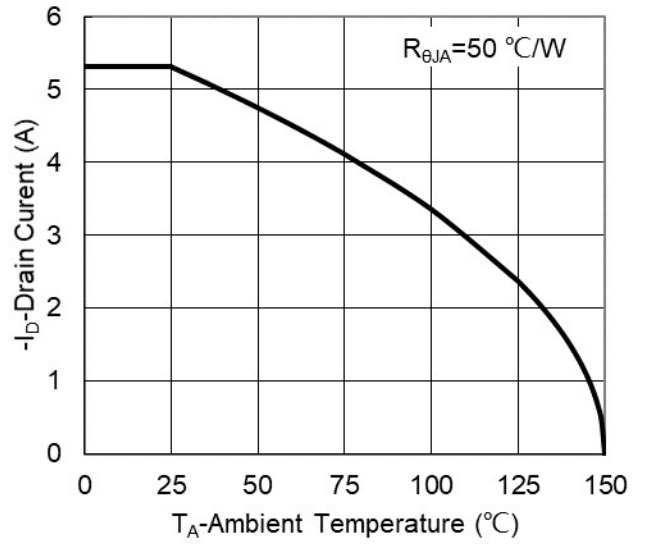


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

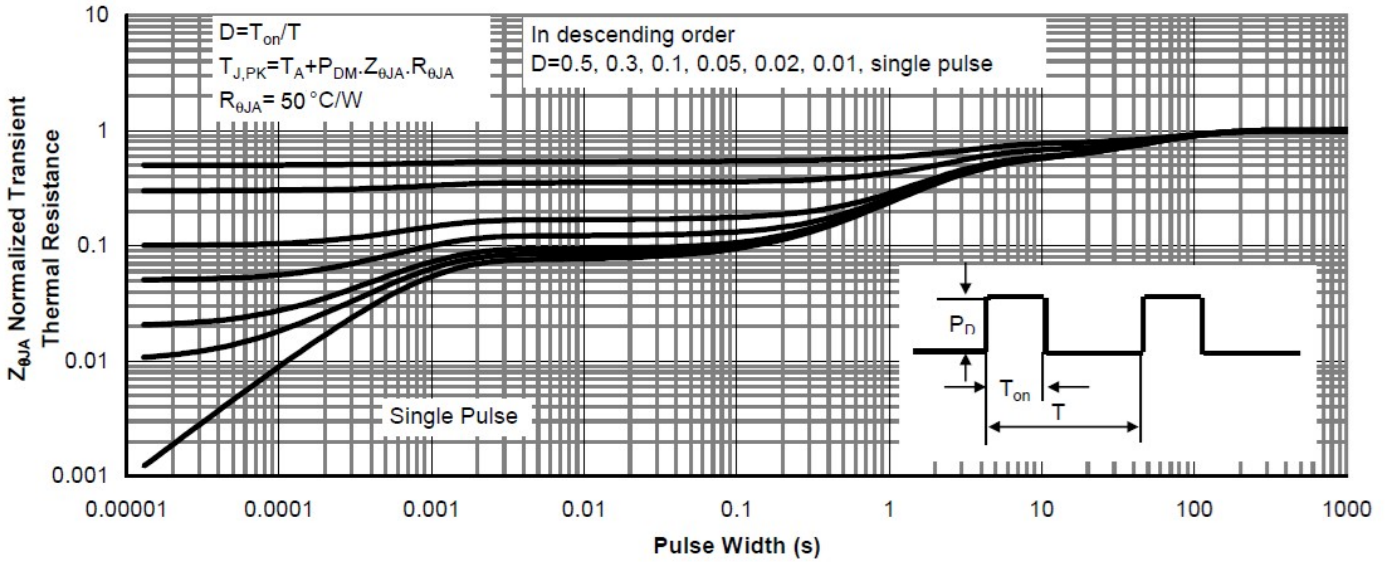
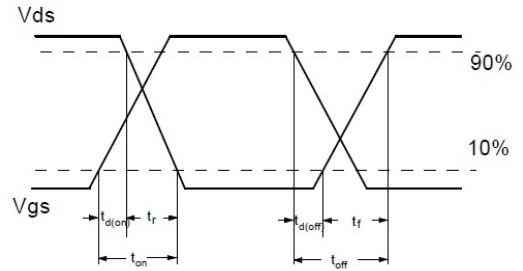


Figure9. Normalized Maximum Transient Thermal Impedance



**Resistive Switching Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**



**Gate Charge Test Circuit & Waveform**

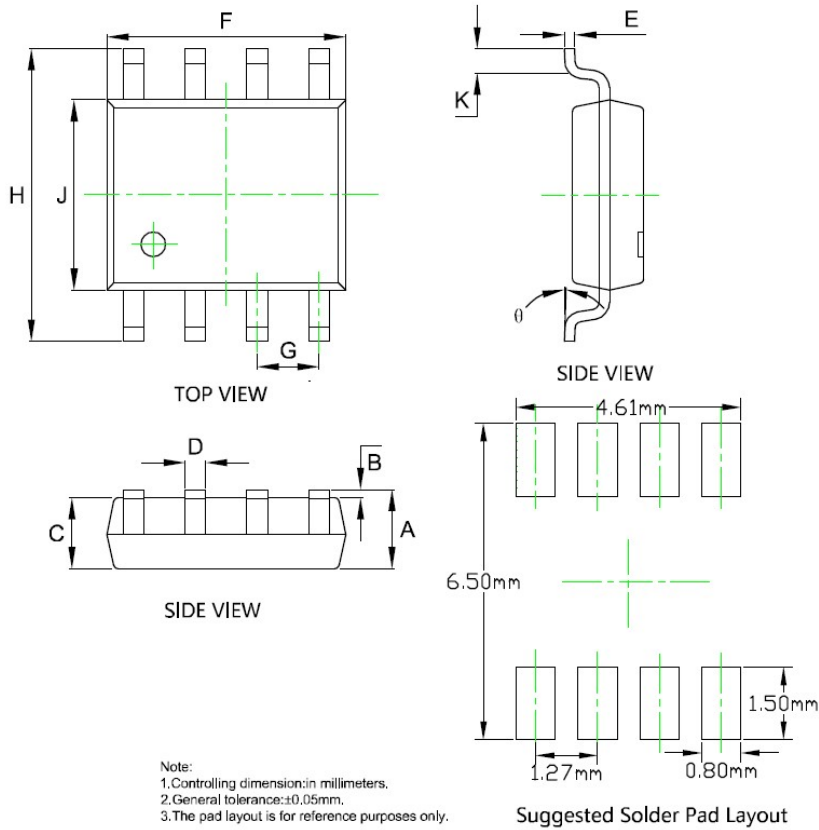


**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**



# YJS9435A

## ■ SOP-8 Package information



| SYMBOL | DIMENSIONS |       |            |       |
|--------|------------|-------|------------|-------|
|        | INCHES     |       | Millimeter |       |
|        | MIN.       | MAX.  | MIN.       | MAX.  |
| A      | 0.053      | 0.069 | 1.350      | 1.750 |
| B      | 0.004      | 0.010 | 0.100      | 0.250 |
| C      | 0.053      | 0.061 | 1.350      | 1.550 |
| D      | 0.013      | 0.020 | 0.330      | 0.510 |
| E      | 0.007      | 0.010 | 0.170      | 0.250 |
| F      | 0.189      | 0.197 | 4.800      | 5.000 |
| G      | 0.050BSC   |       | 1.270BSC   |       |
| H      | 0.228      | 0.244 | 5.800      | 6.200 |
| J      | 0.150      | 0.157 | 3.800      | 4.000 |
| K      | 0.016      | 0.050 | 0.400      | 1.270 |
| θ      | 0°         | 8°    | 0°         | 8°    |



## YJS9435A

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