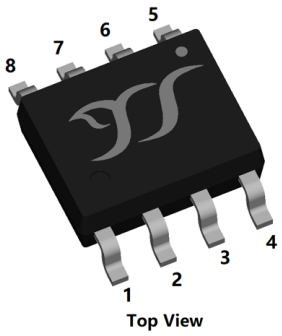
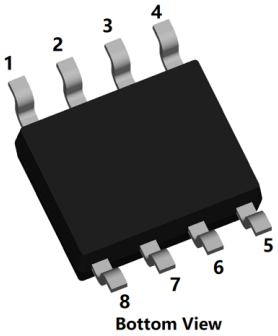
P-Channel Enhancement Mode Field Effect Transistor

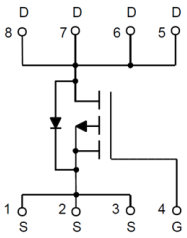


Top View



Bottom View

SOP-8



Product Summary

- V_{DS} -30V
- I_D -18A
- $R_{DS(ON)}$(at V_{GS}=-20V) ＜5.5mohm
- $R_{DS(ON)}$(at V_{GS}=-10V) ＜6.0mohm
- $R_{DS(ON)}$(at V_{GS}=-4.5V) ＜10mohm

General Description

- Trench Power LV MOSFET technology
- High density cell design for Low $R_{DS(ON)}$
- High Speed switching
- Moisture Sensitivity Level 3
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Battery protection
- Power management
- Load switch

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-source Voltage		V_{DS}	-30	V
Gate-source Voltage		V_{GS}	±25	V
Drain Current	T_A=25℃ @ Steady State	I_D	-18	A
	T_A=70℃ @ Steady State		-14.4	
Pulsed Drain Current [A]		I_{DM}	-72	A
Single Pulse Avalanche Energy [B]		E_{AS}	136	mJ
Total Power Dissipation @ T_A=25℃ [C]		P_D	3.4	W
Thermal Resistance Junction-to-Ambient @ Steady State [D]		$R_{\theta JA}$	36.7	℃/ W
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJS4409A	F2	Q4409	4000	8000	64000	13“ reel

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=-250μA	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-30V,V_{GS}=0V,T_C=25℃			-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±25V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250μA	-1.0	-1.5	-2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= -20V, I_D=-18A		4.5	5.5	mΩ
		V_{GS}= -10V, I_D=-15A		5.1	6.0	
		V_{GS}= -6V, I_D=-10A		7.0	8.5	
		V_{GS}= -4.5V, I_D=-10A		7.5	10	
Diode Forward Voltage	V_{SD}	I_S=-18A,V_{GS}=0V		-0.8	-1.2	V
Gate resistance	R_G	f=1MHz	-	3	-	Ω
Maximum Body-Diode Continuous Current	I_S		-	-	-18	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=-15V,V_{GS}=0V,f=1MHZ		4850		pF
Output Capacitance	C_{oss}			674		
Reverse Transfer Capacitance	C_{rss}			624		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=-10V,V_{DS}=-15V,I_D=-12A		77.2		nC
Gate Source Charge	Q_{gs}			13.5		
Gate Drain Charge	Q_{gd}			17.3		
Reverse Recovery Charge	Q_{rr}	I_F= -12A, di/dt=100A/us		14.0		
Reverse Recovery Time	t_{rr}			30		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-10V,V_{DD}=-15V, I_D=-1A, R_{GEN}=2.5Ω		16		
Turn-on Rise Time	t_r			21		
Turn-off Delay Time	$t_{D(off)}$			105		
Turn-off Fall Time	t_f			64		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

B. $R_{\theta JA}$ is the sum of the junction-to-lead and lead-to-ambient thermal resistance, where the lead thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JL}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ Typical Performance Characteristics

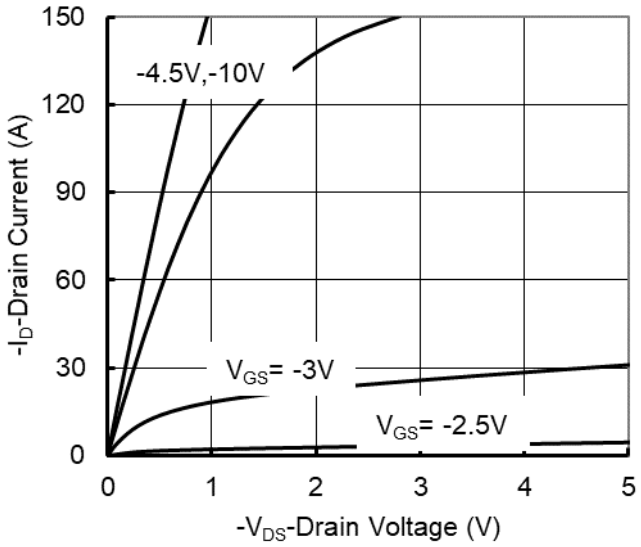


Figure 1. Output Characteristics

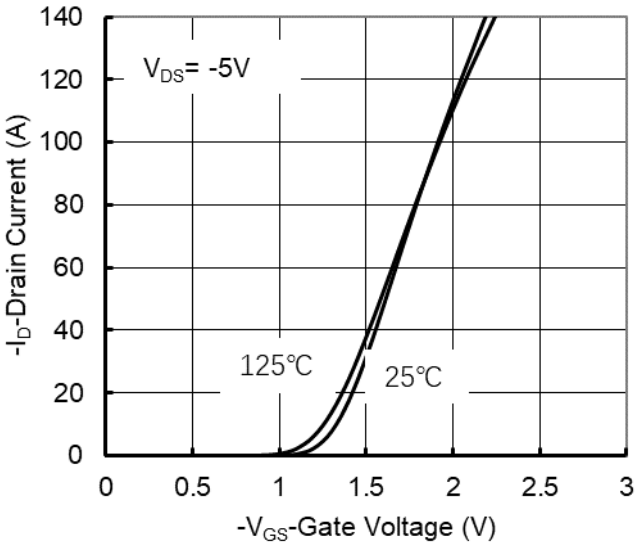


Figure 2. Transfer Characteristics

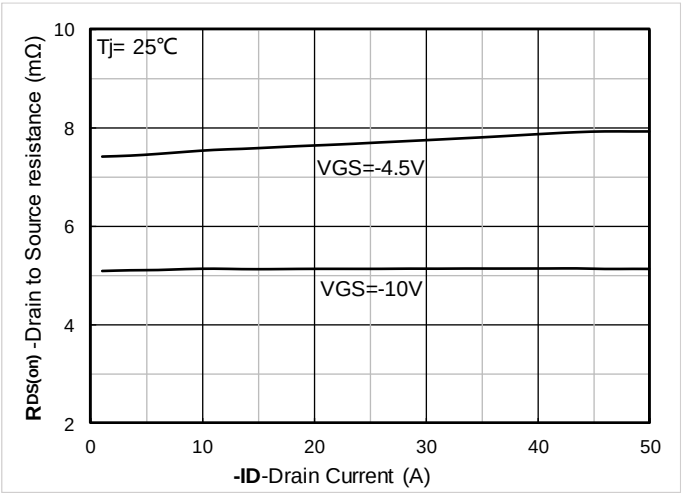


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

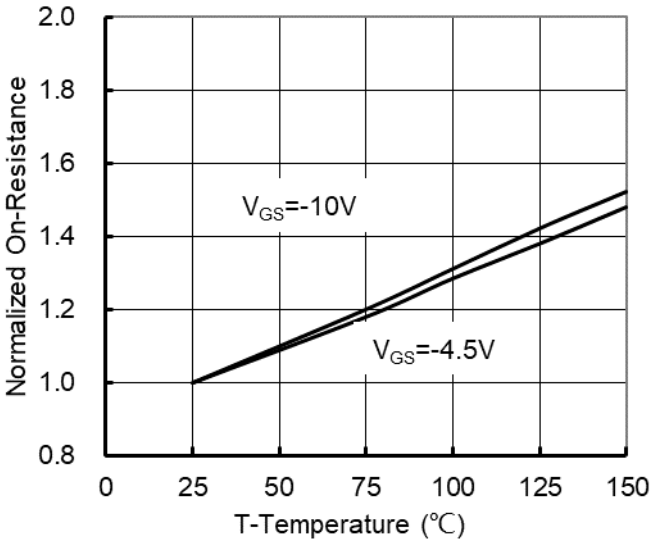


Figure 4. On-Resistance vs. Junction Temperature

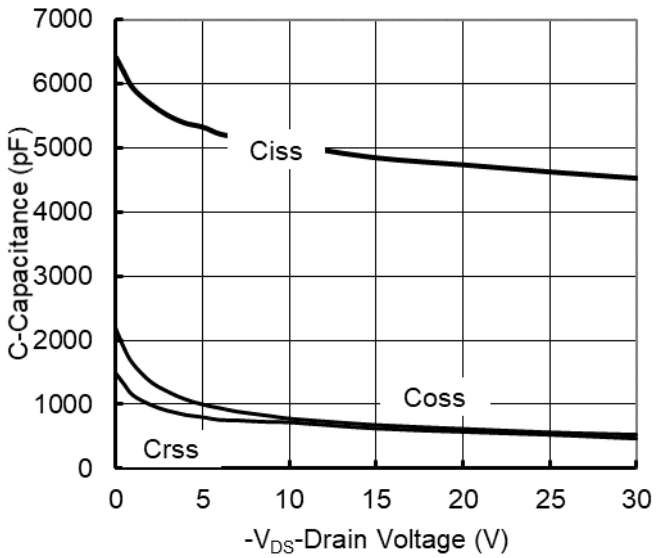


Figure 5. Capacitance Characteristics

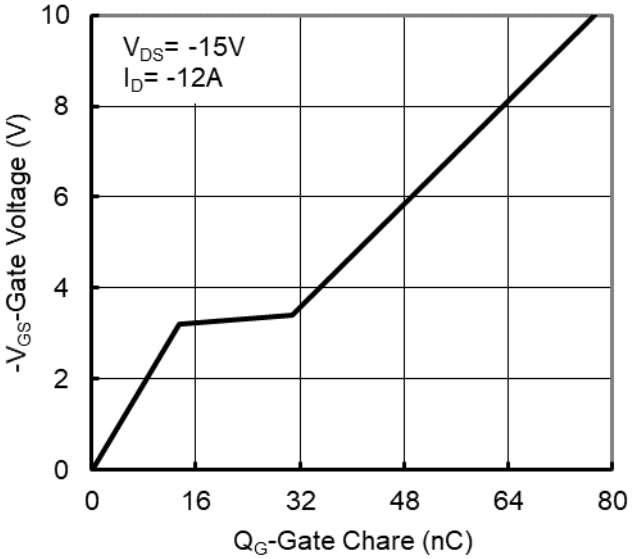


Figure 6. Gate Charge

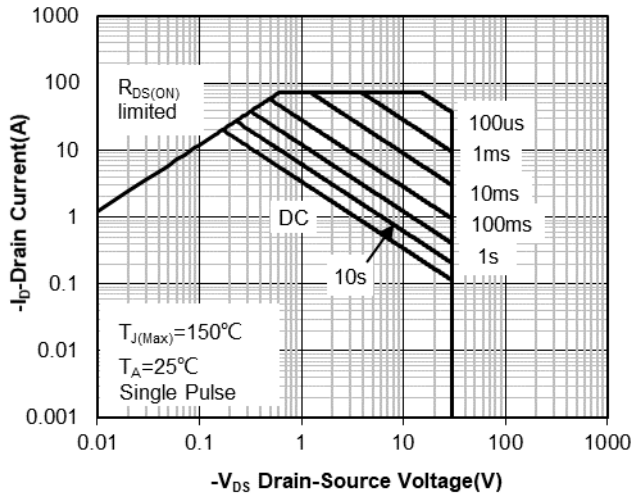


Figure 7. Safe Operation Area

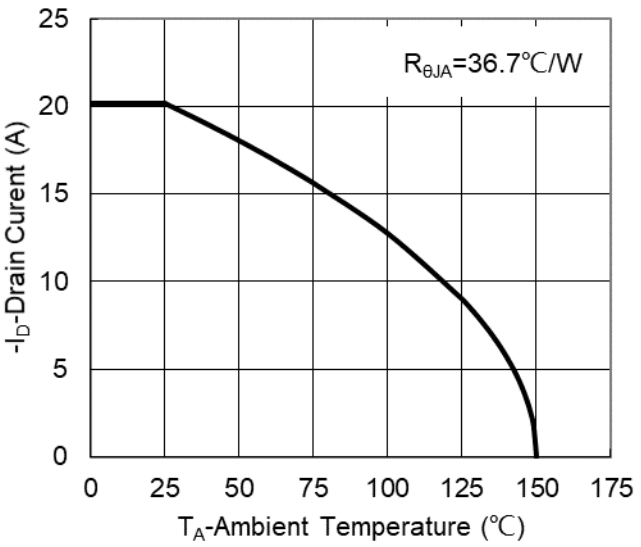


Figure 8. Maximum Continuous Drain Current vs Ambient Temperature

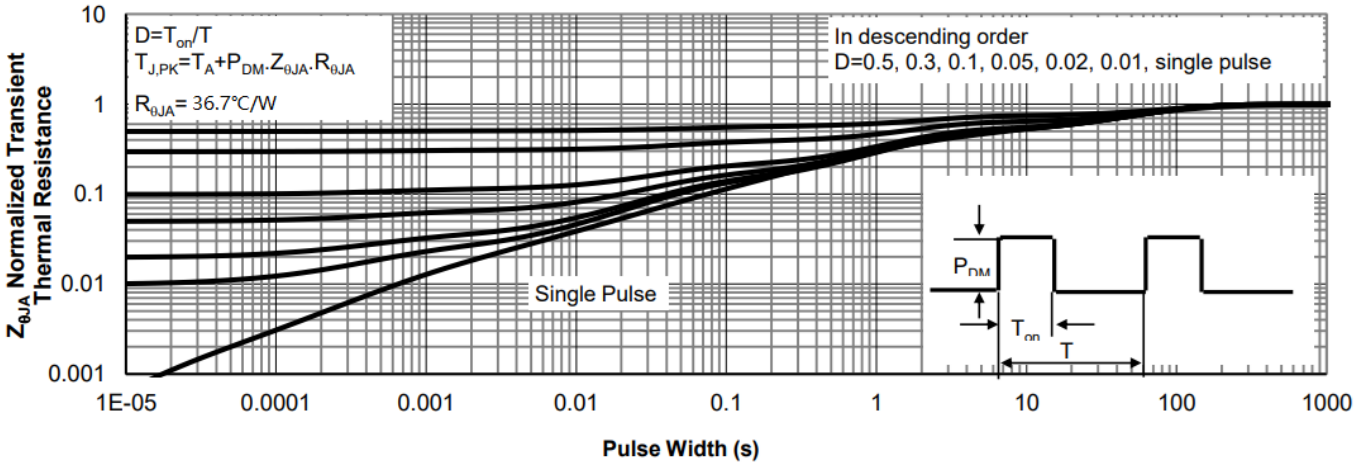
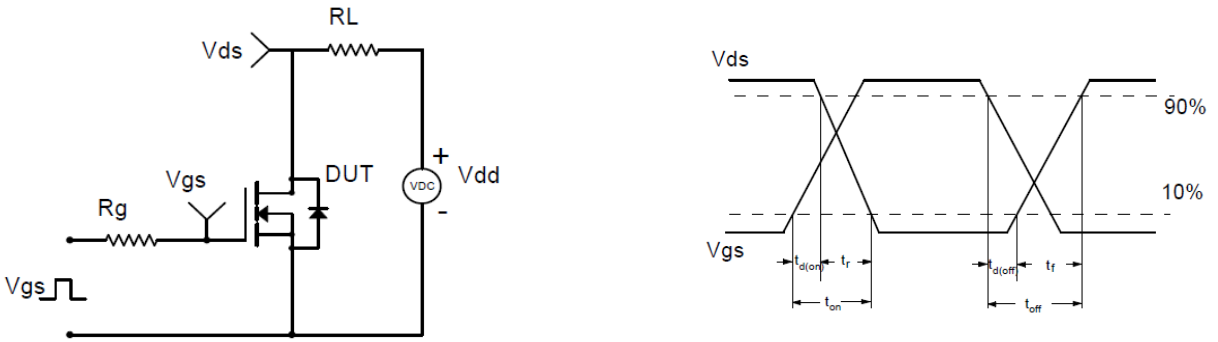
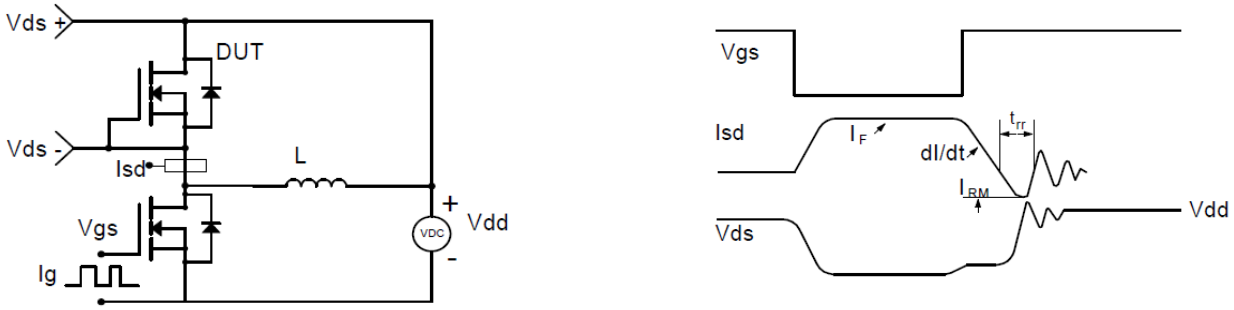


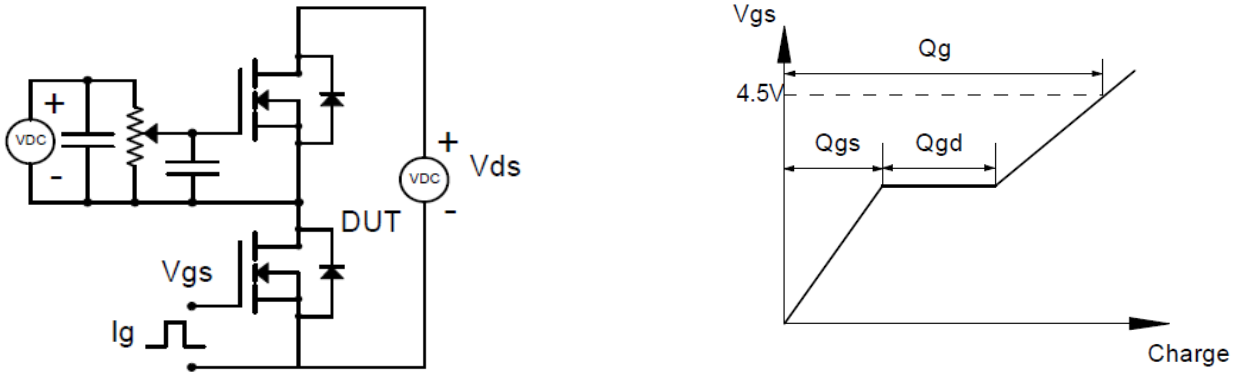
Figure 9. Normalized Maximum Transient Thermal Impedance



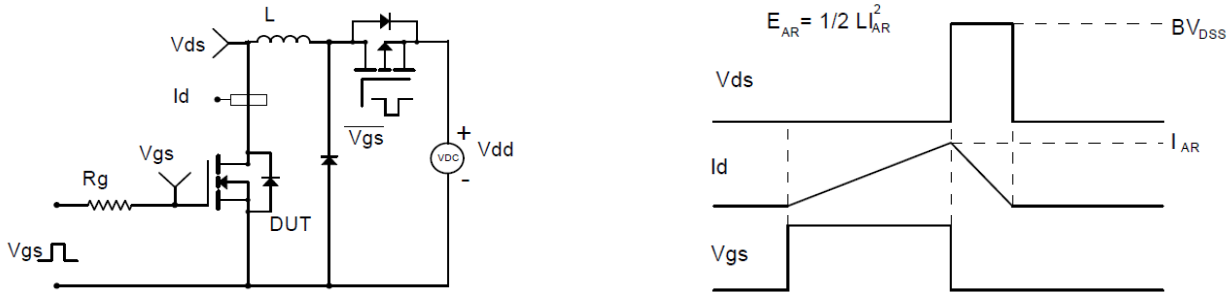
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

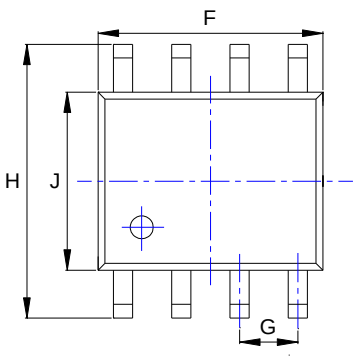


Gate Charge Test Circuit & Waveform

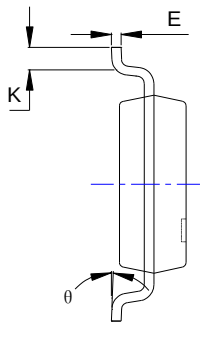


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

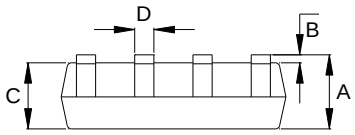
■ SOP-8 Package information



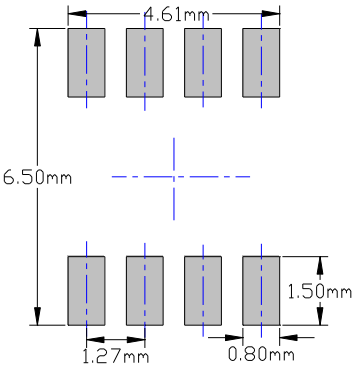
TOP VIEW



SIDE VIEW



SIDE VIEW



Suggested Solder Pad Layout

DIMENSIONS				
SYMBOL	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.053	0.069	1.350	1.750
B	0.004	0.010	0.100	0.250
C	0.053	0.061	1.350	1.550
D	0.013	0.020	0.330	0.510
E	0.007	0.010	0.170	0.250
F	0.189	0.197	4.800	5.000
G	0.050BSC		1.270BSC	
H	0.228	0.244	5.800	6.200
J	0.150	0.157	3.800	4.000
K	0.016	0.050	0.400	1.270
θ	0°	8°	0°	8°

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:+/-0.05mm.
3.The pad layout is for reference purposes only.

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