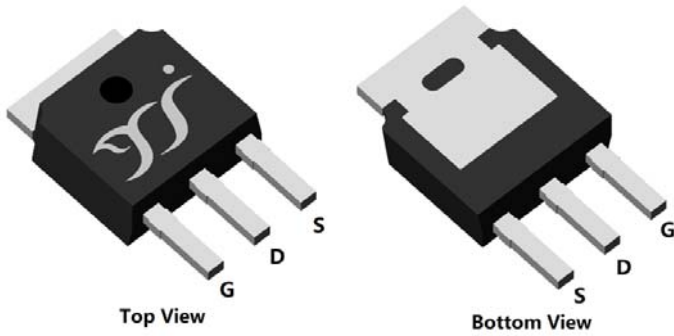
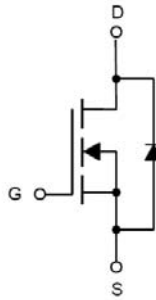


## N-Channel Enhancement Mode Field Effect Transistor



TO-251



### Product Summary

- $V_{DS}$  60V
- $I_D$  20A
- $R_{DS(ON)}$  (at  $V_{GS}=10V$ ) <43mohm
- $R_{DS(ON)}$  (at  $V_{GS}=4.5V$ ) <47mohm
- 100% EAS Tested
- 100%  $\nabla V_{DS}$  Tested

### General Description

- Trench Power MV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

### Applications

- DC-DC Converters
- Power management functions
- Backlighting

### ■ Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source Voltage	$V_{DS}$	60	V
Gate-source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current	$I_D$	$T_C=25^\circ\text{C}$	20
		$T_C=100^\circ\text{C}$	12
Pulsed Drain Current <sup>A</sup>	$I_{DM}$	60	A
Total Power Dissipation	$P_D$	$T_C=25^\circ\text{C}$	28
		$T_C=100^\circ\text{C}$	11
Single Pulse Avalanche Energy <sup>B</sup>	$E_{AS}$	30.25	mJ
Thermal Resistance Junction-to-Case <sup>C</sup>	$R_{\theta JC}$	4.4	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55~+150	$^\circ\text{C}$

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJR20N06A	B1	YJR20N06A	75	/	22500	Tube



# YJR20N06A

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =250μA	60			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V	T <sub>J</sub> =25°C		1	μA
			T <sub>J</sub> =150°C		100	
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0	1.5	2.5	V
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> =20A		29	43	mΩ
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> =10A		31	47	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =10A, V <sub>GS</sub> =0V		0.8	1.2	V
Maximum Body-Diode Continuous Current	I <sub>S</sub>				20	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V, f=1MHZ		1018		pF
Output Capacitance	C <sub>oss</sub>			70		
Reverse Transfer Capacitance	C <sub>rss</sub>			62		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =30V, I <sub>D</sub> =10A		26		nC
Gate-Source Charge	Q <sub>gs</sub>			5.4		
Gate-Drain Charge	Q <sub>gd</sub>			6.5		
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =20A, di/dt=500A/us		11.7		
Reverse Recovery Time	t <sub>rr</sub>			23		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =10V, V <sub>DD</sub> =30V, I <sub>D</sub> =2A, R <sub>L</sub> =1Ω R <sub>GEN</sub> =3Ω		10		ns
Turn-on Rise Time	t <sub>r</sub>			20		
Turn-off Delay Time	t <sub>D(off)</sub>			29		
Turn-off fall Time	t <sub>f</sub>			22		

A. Pulse Test: Pulse Width≤300us, Duty cycle ≤2%.

B. T<sub>J</sub>=25°C, V<sub>DD</sub>=40V, V<sub>G</sub>=10V, L=0.5mH, I<sub>AS</sub>=11A

C. R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design, while R<sub>θJA</sub> is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



■ Typical Performance Characteristics

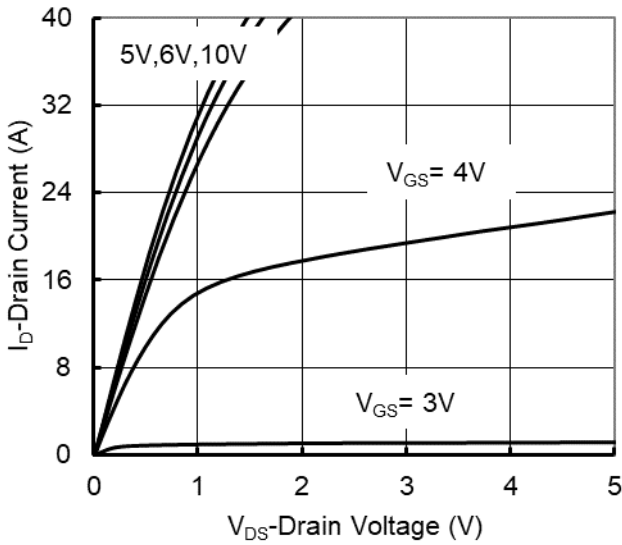


Figure 1. Output Characteristics

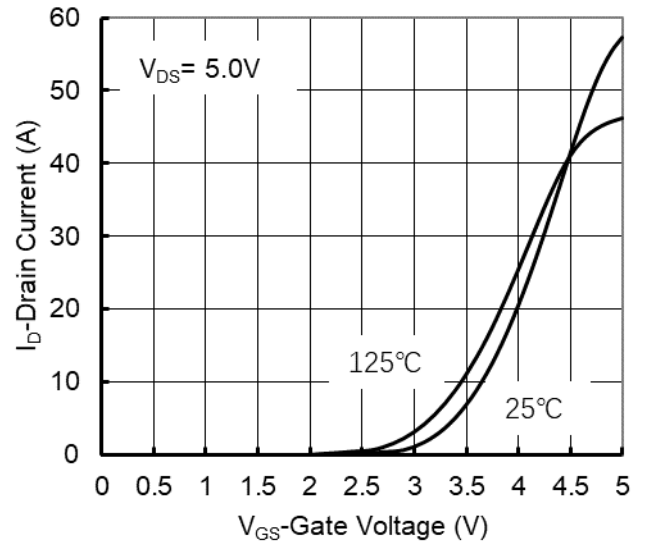


Figure 2. Transfer Characteristics

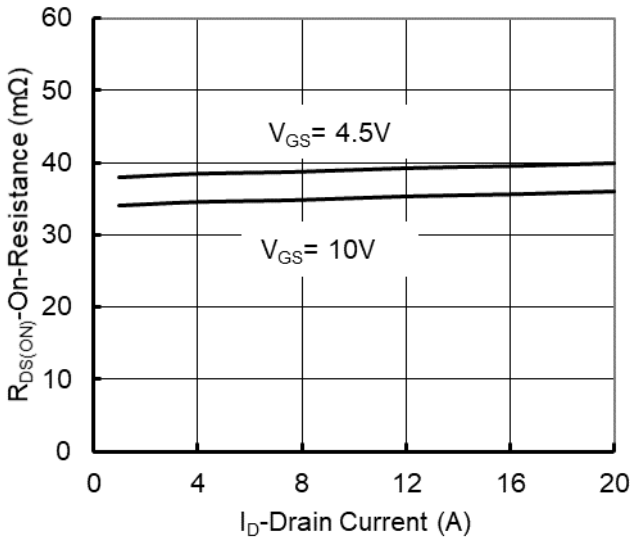


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

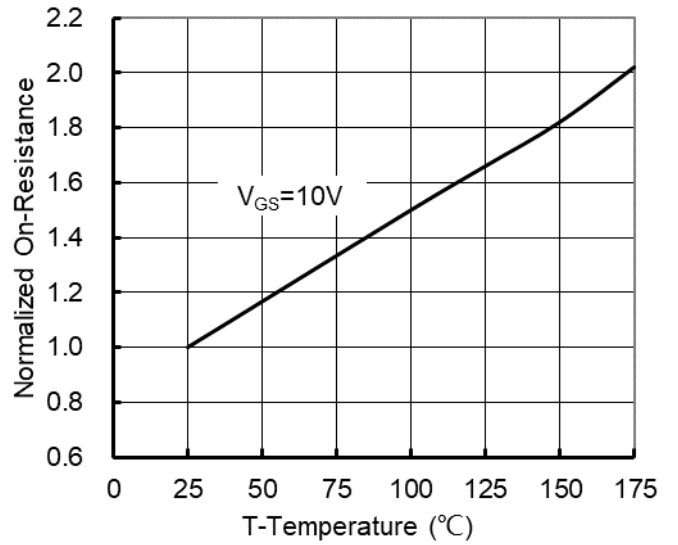


Figure 4. On-Resistance vs. Junction Temperature

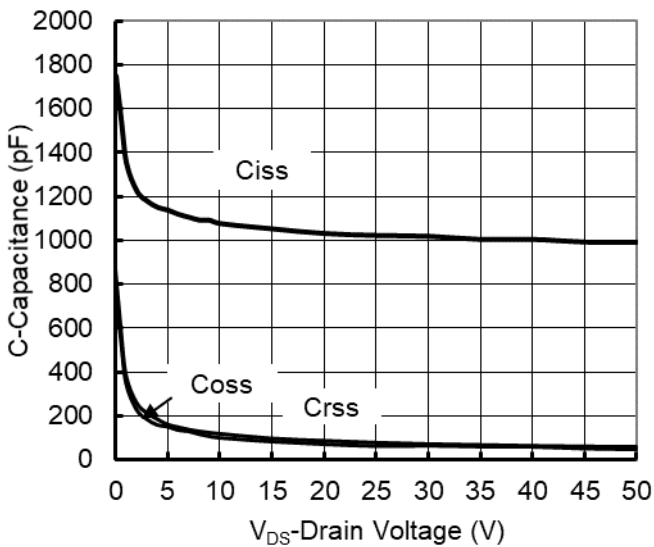


Figure 5. Capacitance Characteristics

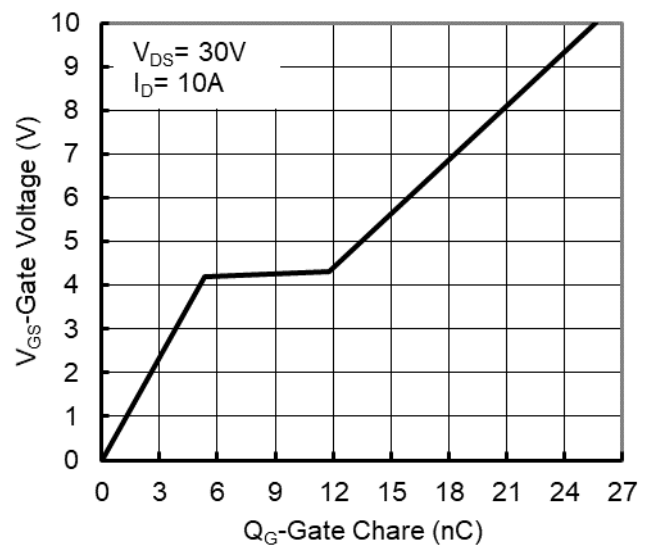


Figure 6. Gate Charge



# YJR20N06A

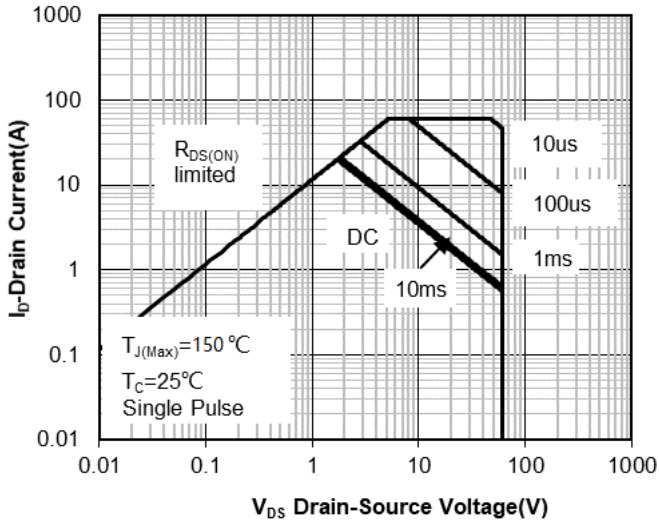


Figure 7. Safe Operation Area

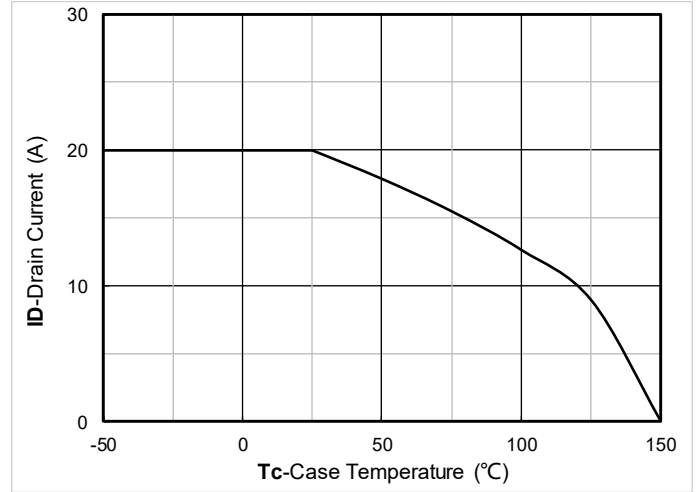


Figure 8. Maximum Continuous Drain Current vs Case Temperature

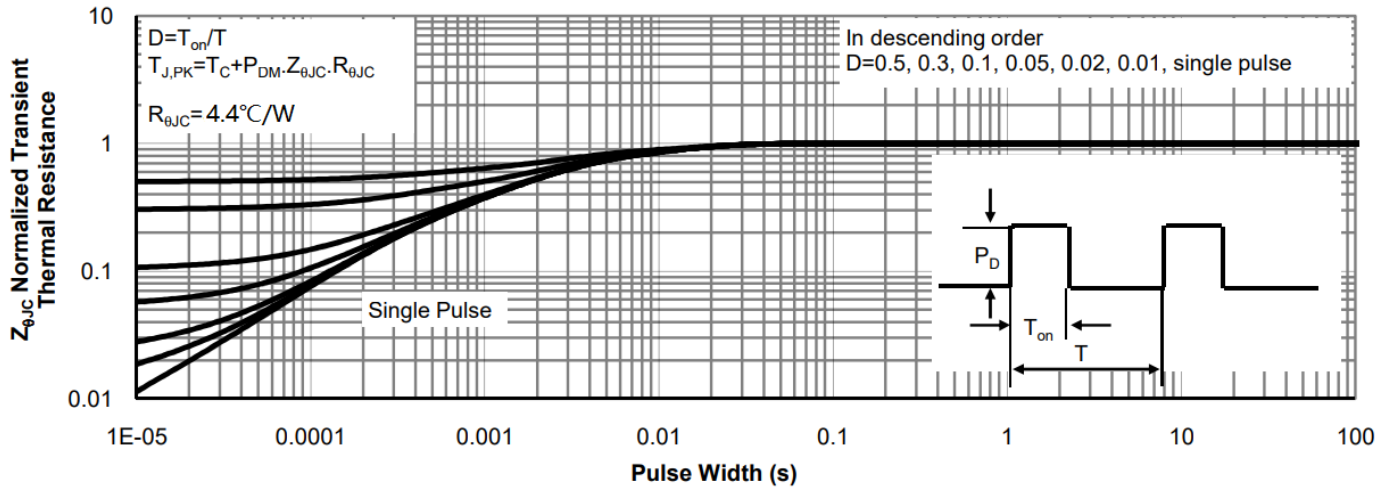
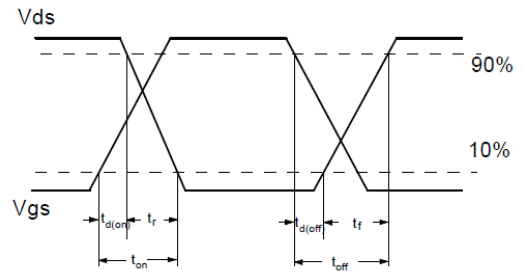
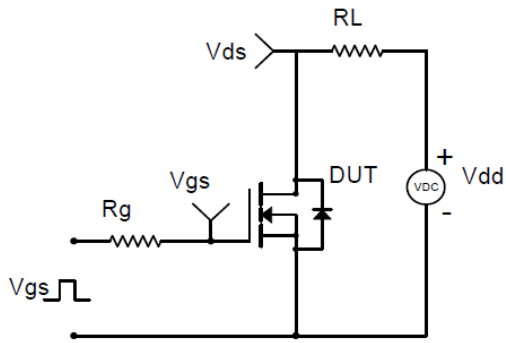
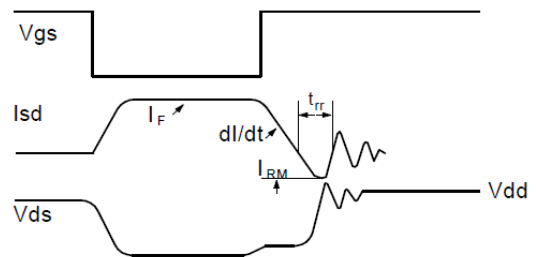
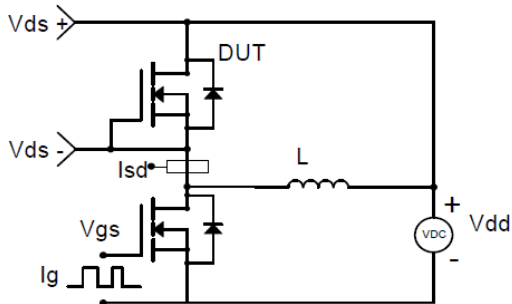


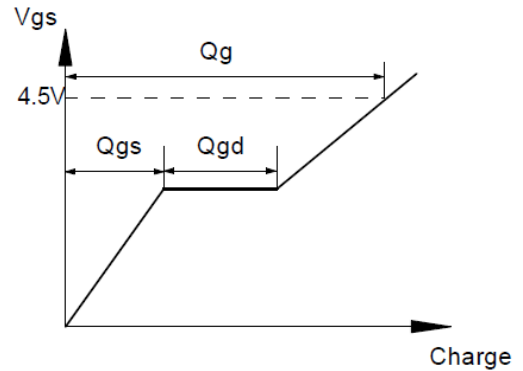
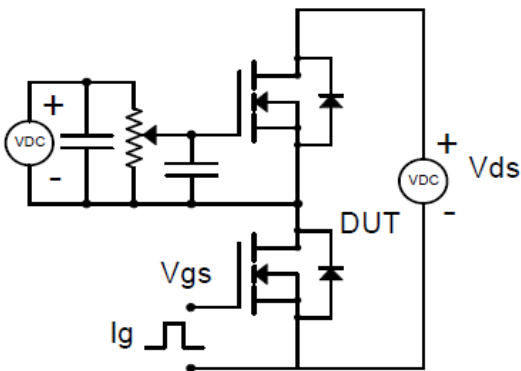
Figure 9. Normalized Maximum Transient Thermal Impedance



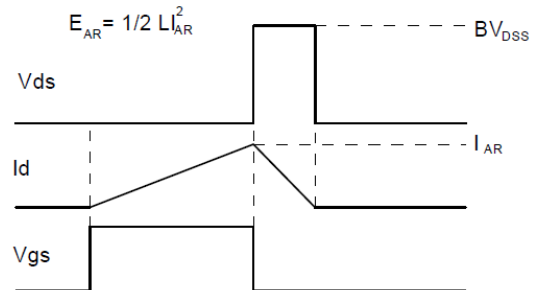
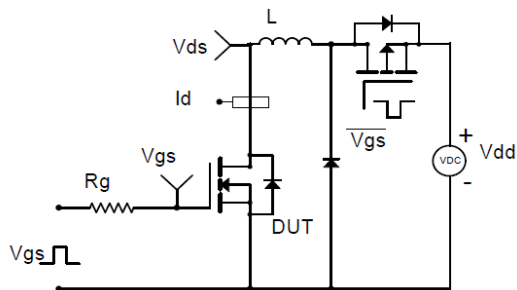
**Resistive Switching Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**



**Gate Charge Test Circuit & Waveform**

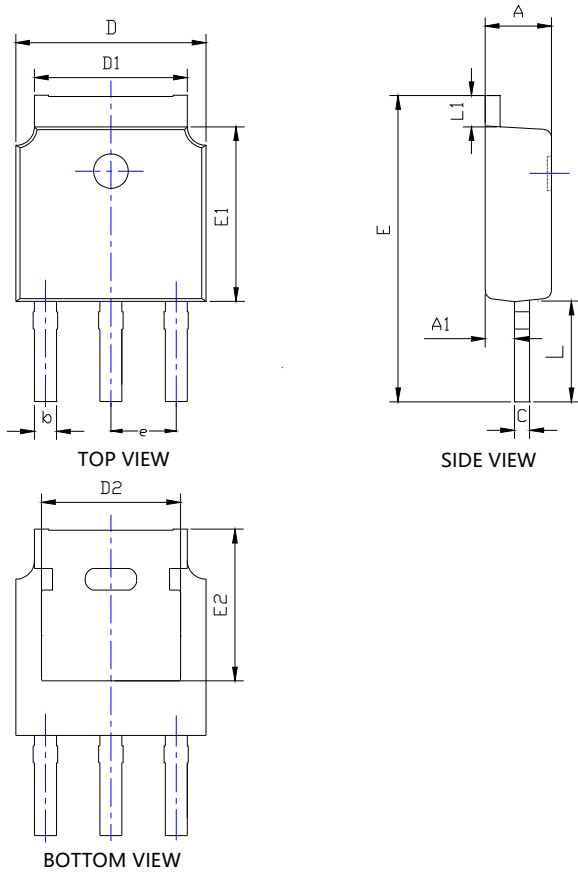


**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**



# YJR20N06A

## ■ TO-251 Package Information



SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.087	0.094	2.200	2.400
A1	0.035	0.043	0.900	1.100
b	0.026	0.034	0.660	0.860
c	0.018	0.023	0.460	0.580
D	0.256	0.264	6.500	6.700
D1	0.203	0.215	5.150	5.450
D2	0.181	0.195	4.600	4.950
E	0.409	0.453	10.400	11.500
E1	0.236	0.244	6.000	6.200
E2	0.213REF		5.400REF	
e	0.090BSC		2.286BSC	
L	0.138	0.169	3.500	4.300
L1	0.035	0.050	0.900	1.270

NOTE:  
 1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.  
 2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.



## YJR20N06A

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