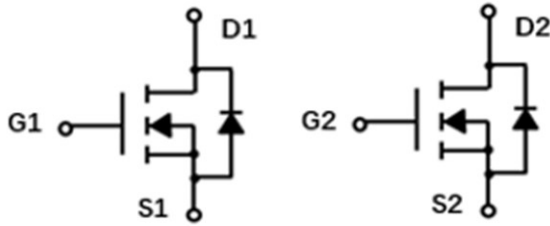
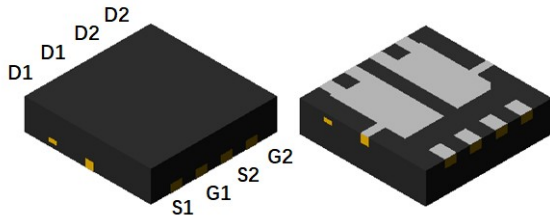


## N-Channel Enhancement Mode Field Effect Transistor

### DFN3.3X3.3



### Product Summary

- $V_{DS}$  30 V
- $I_D$  12 A
- $R_{DS(ON)}$  (at  $V_{GS}=10V$ ) < 16 mohm
- $R_{DS(ON)}$  (at  $V_{GS}=4.5V$ ) < 30 mohm
- 100% UIS Tested
- 100%  $\nabla V_{DS}$  Tested

### General Description

- Trench Power LV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$

### Applications

- High current load applications
- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

### ■ Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source Voltage	$V_{DS}$	30	V
Gate-source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current	$I_D$	$T_C=25^\circ\text{C}$	12
		$T_C=100^\circ\text{C}$	7.6
Pulsed Drain Current <sup>A</sup>	$I_{DM}$	48	A
Single Pulse Avalanche Energy <sup>B</sup>	$E_{AS}$	19	mJ
Total Power Dissipation	$P_D$	12	W
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	6.0	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction-to-ambient	$R_{\theta JA}$	40	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55~+150	$^\circ\text{C}$

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQD12N03A	F1	Q12N03A	5000	10000	100000	13" reel



# YJQD12N03A

## ■ Electrical Characteristics ( $T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	30			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=30V, V_{GS}=0V$			1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$			$\pm 100$	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.5	2.5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=10A$		12.5	16	m $\Omega$
		$V_{GS}=4.5V, I_D=8A$		24.5	30	
Diode Forward Voltage	$V_{SD}$	$I_S=12A, V_{GS}=0V$		0.85	1.2	V
<b>Dynamic Parameters</b>						
Input Capacitance	$C_{iss}$	$V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$		3851		pF
Output Capacitance	$C_{oss}$			444		
Reverse Transfer Capacitance	$C_{rss}$			316		
<b>Switching Parameters</b>						
Total Gate Charge	$Q_g$	$V_{GS}=4.5V, V_{DS}=10V, I_D=20A$		45.3		nC
Gate-Source Charge	$Q_{gs}$			7.5		
Gate-Drain Charge	$Q_{gd}$			11.1		
Reverse Recovery Charge	$Q_{rr}$	$I_F=20A, di/dt=100A/us$		6.9		
Reverse Recovery Time	$t_{rr}$			27		
Turn-on Delay Time	$t_{D(on)}$	$V_{GS}=4.5V, V_{DD}=10V, R_L=0.5\Omega, R_{GEN}=3\Omega$		22		ns
Turn-on Rise Time	$t_r$			107		
Turn-off Delay Time	$t_{D(off)}$			86		
Turn-off fall Time	$t_f$			115		

A. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty cycle  $\leq 2\%$ .

B.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design, while  $R_{\theta JA}$  is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



## ■ Typical Performance Characteristics

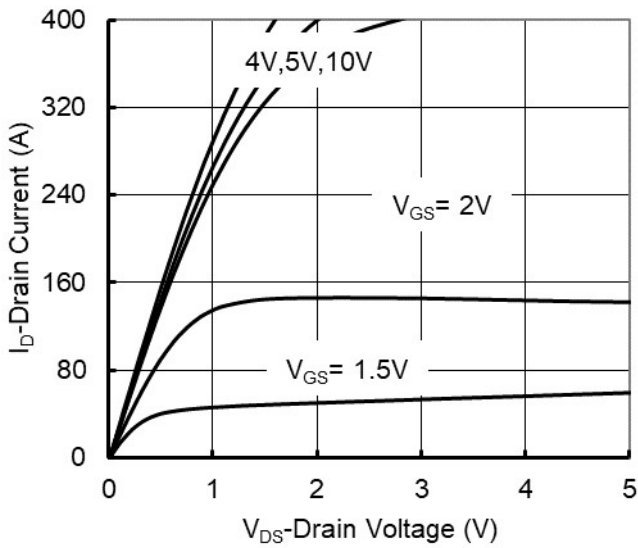


Figure 1. Output Characteristics

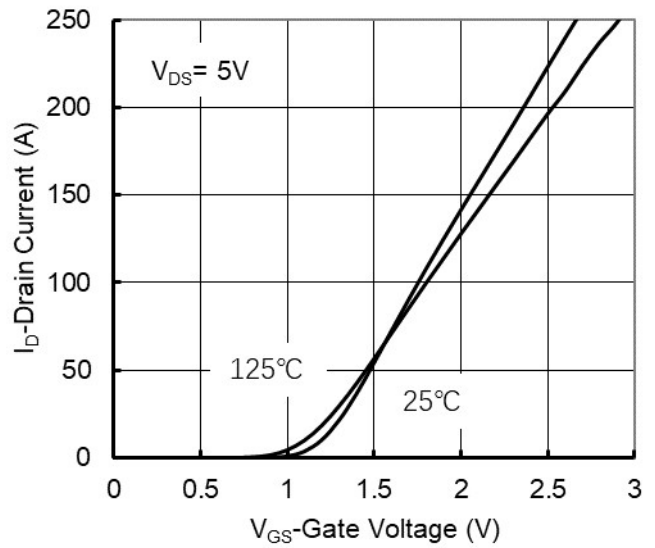


Figure 2. Transfer Characteristics

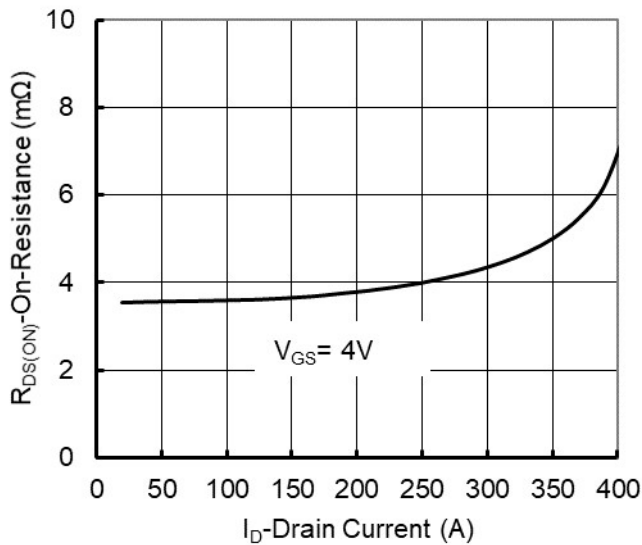


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

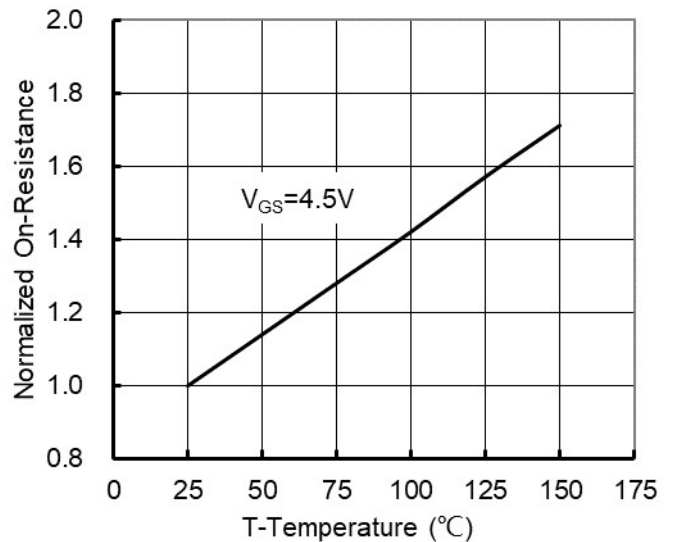


Figure 4. On-Resistance vs. Junction Temperature

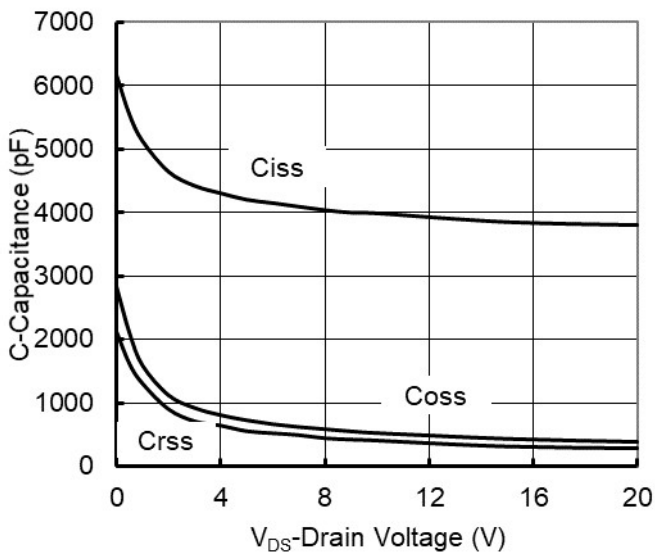


Figure 5. Capacitance Characteristics

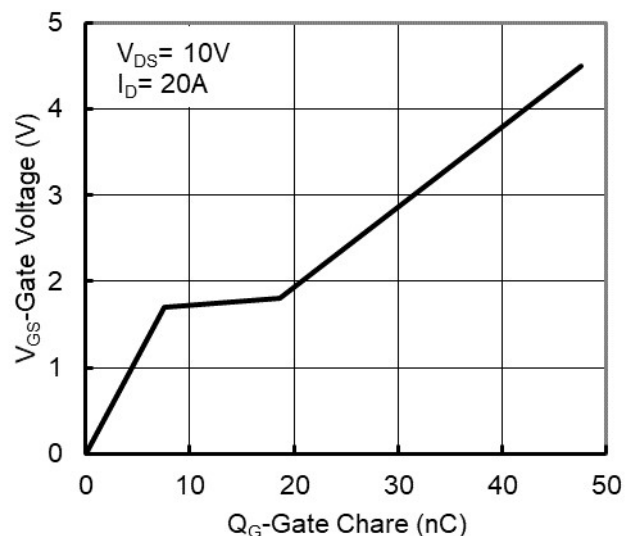


Figure 6. Gate Charge

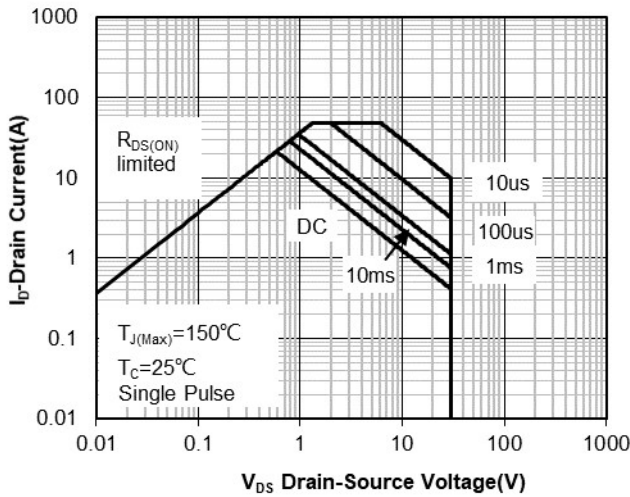


Figure 7. Safe Operation Area

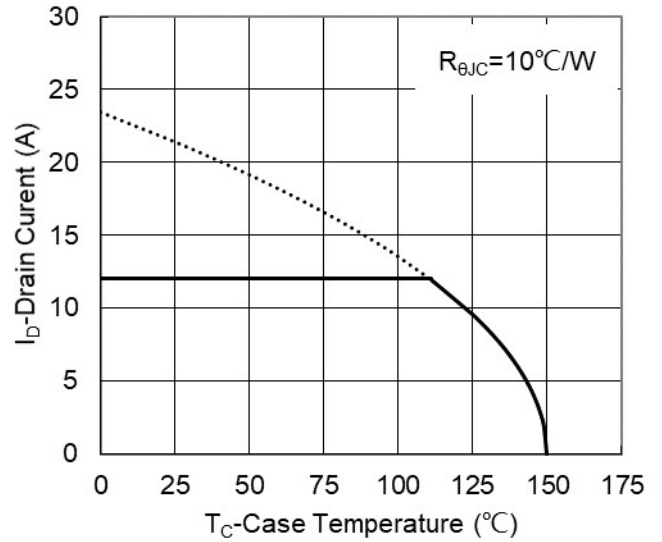


Figure 8. Maximum Continuous Drain Current vs Case Temperature

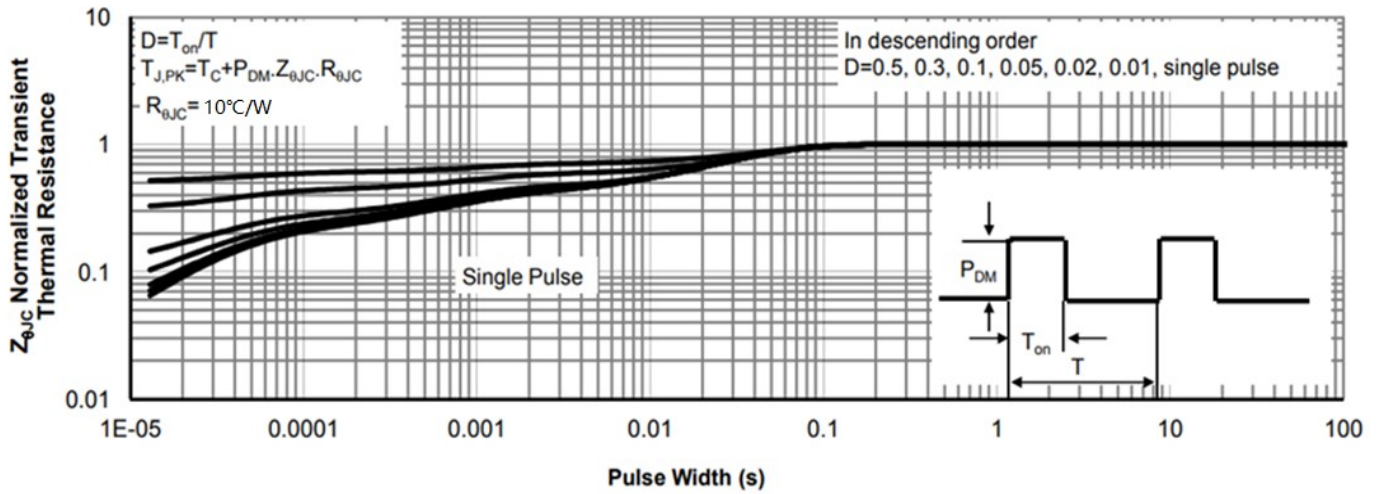
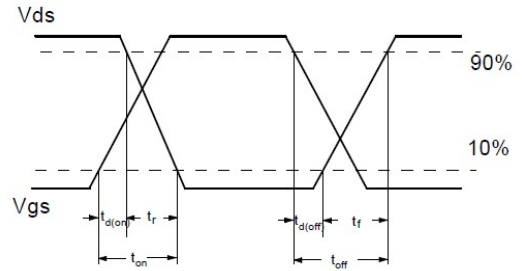
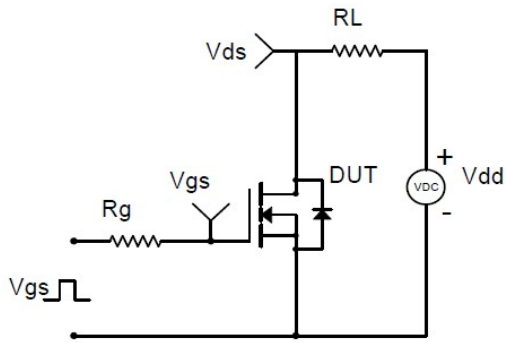
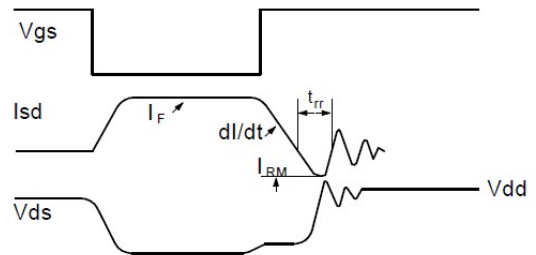
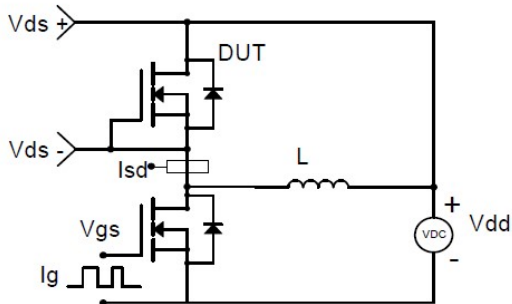


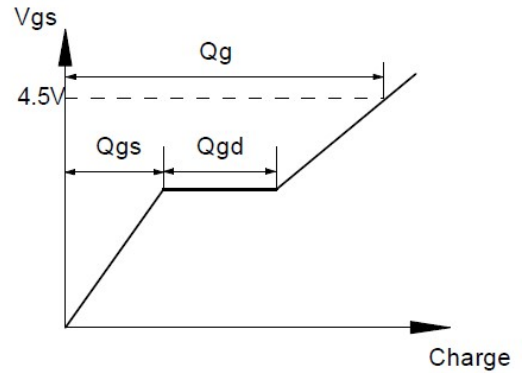
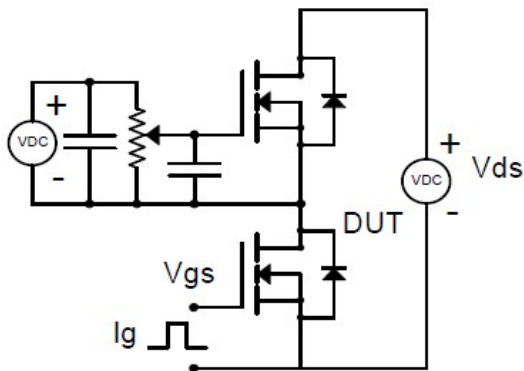
Figure 9. Normalized Maximum Transient Thermal Impedance



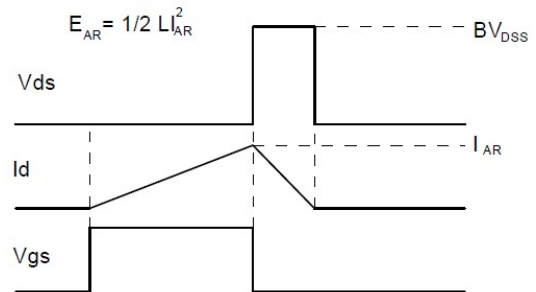
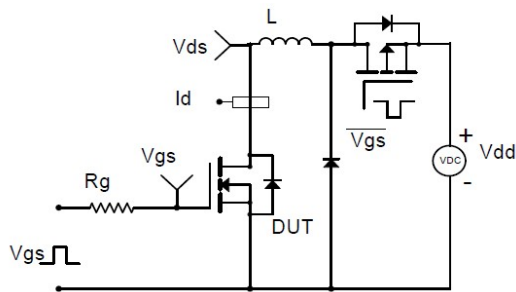
**Resistive Switching Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**



**Gate Charge Test Circuit & Waveform**

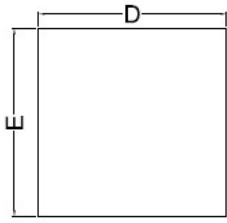


**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**

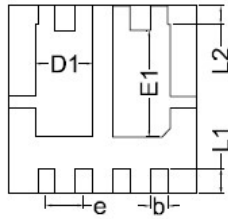


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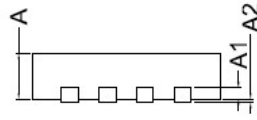
## ■ DFN3.3X3.3 Package Information



Top View  
正面视图

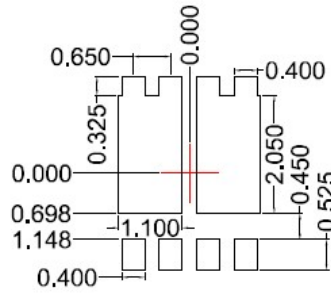


Bottom View  
背面视图



Side View  
侧面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	0.90	1.00	1.10
E1	1.75	1.85	1.95
L1	0.325	0.425	0.525
L2	0.325 BSC		
b	0.20	0.30	0.40
e	0.65 BSC		



Suggested Solder Pad Layout  
Top View

Note:

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.10$ mm.
3. The pad layout is for reference purposes only.



## YJQD12N03A

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