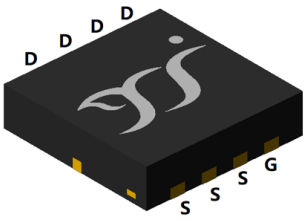
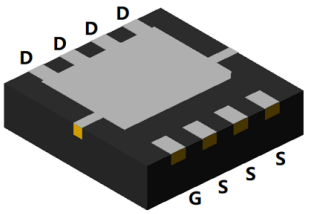
P-Channel Enhancement Mode Field Effect Transistor

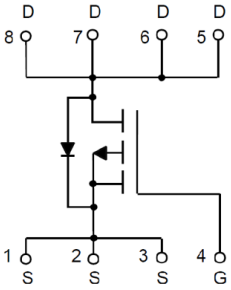


Top View



Bottom View

DFN3333-8L



Product Summary

- V_{DS} -30V
- I_D -50A
- $R_{DS(ON)}$(at VGS=-10V) ＜6.2mohm
- $R_{DS(ON)}$(at VGS=-4.5V) ＜11mohm
- 100% EAS Tested

General Description

- Trench Power LV MOSFET technology
- High Power and current handing capability
- Moisture Sensitivity Level 3
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- High current load applications
- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	-30	V
Gate-source Voltage		V_{GS}	±25	V
Drain Current	T_A=25℃	I_D	14	A
	T_A=70℃		11	
	T_C=25℃		-50	
	T_C =70℃		-31	
Pulsed Drain Current [A]		I_{DM}	-200	A
Avalanche energy [D]		EAS	400	mJ
Total Power Dissipation [E]	T_A=25℃	P_D	5.2	W
	T_A=70℃		1.6	
	T_C=25℃		75	
	T_C =70℃		47	
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

■Thermal resistance

Parameter		Symbol	Typ	Max	Units
Junction to Ambient @Maximum[B]	t≤10S	$R_{\theta JA}$	18	24	℃/W
Junction to Ambient @Maximum[BC]	Steady-State		36	50	
Junction to Case @Maximum	Steady-State	$R_{\theta JC}$	1	1.7	

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ50P03A	F1	Q50P03A	5000	10000	100000	13“ reel

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=-250μA	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-30V,V_{GS}=0V			-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±25V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250μA	-1.2	-1.8	-2.8	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= -10V, I_D= -15A		5.0	6.2	mΩ
		V_{GS}= -4.5V, I_D= -10A		6.9	11	
Diode Forward Voltage	V_{SD}	I_S= -15A,V_{GS}=0V			-1.2	V
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=-15V,V_{GS}=0V,f=1MHZ		6464		pF
Output Capacitance	C_{oss}			779		
Reverse Transfer Capacitance	C_{rss}			477		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}= -10V,V_{DS}= -15V,I_D= -20A		111.7		nC
Gate-Source Charge	Q_{gs}			21.1		
Gate-Drain Charge	Q_{gd}			22.9		
Reverse Recovery Chrage	Q_{rr}	I_F=-20A, dI/dt=100A/μs		8.5		
Reverse Recovery Time	t_{rr}			24		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}= -10V,V_{DD}= -15V,R_G=3Ω,R_L= 0.75Ω		15		
Turn-on Rise Time	t_r			79		
Turn-off Delay Time	$t_{D(off)}$			136		
Turn-off fall Time	t_f			80		

A: Pulse Test:Pulse Width≤300us,Duty cycle≤2%.

B. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in^2 FR-4 board with 2oz,Copper,in a still air.environment with T_A =25℃,The Value in any given application depends on the user's specific board design.

C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JC}$ and lead to ambient.

D. T_J=25℃, V_{DD}=-30V, V_G=-10V, R_G=25Ω, L=2mH, IAS=-20A.

E. P_d is based on max. junction temperature, using junction-case and junction-ambient thermal resistance.

■ Typical Performance Characteristics

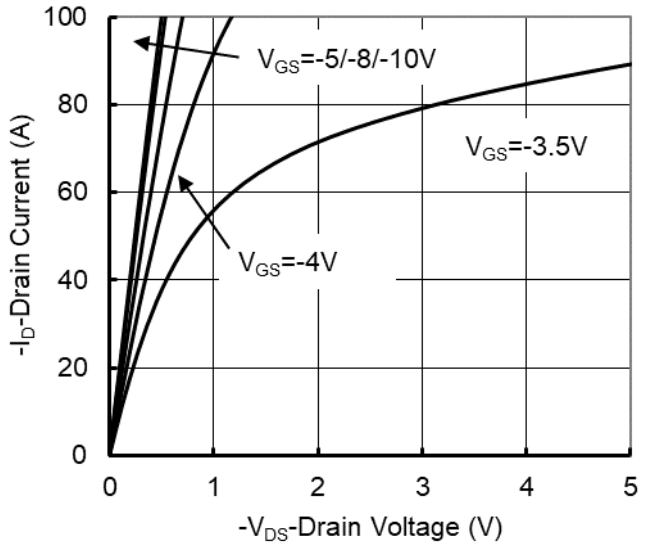


Figure1. Output Characteristics

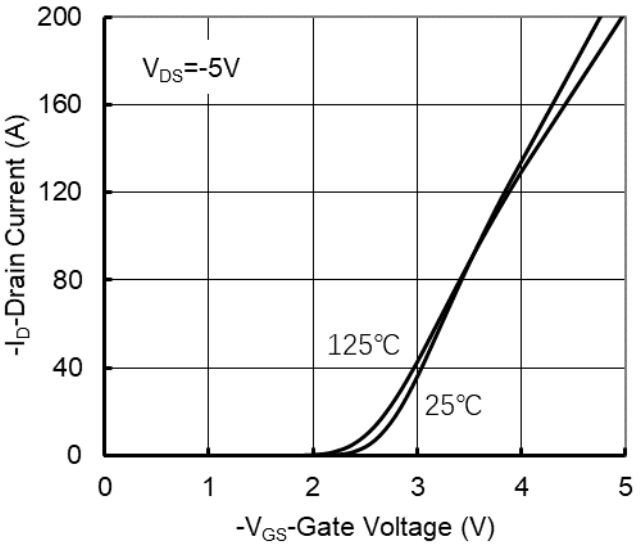


Figure2. Transfer Characteristics

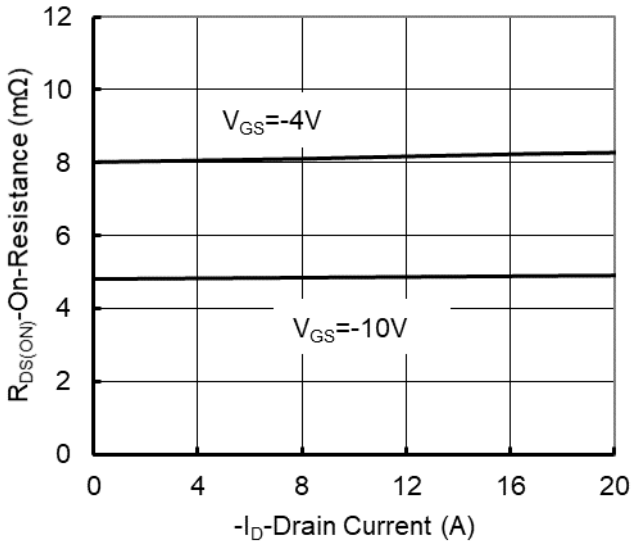


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

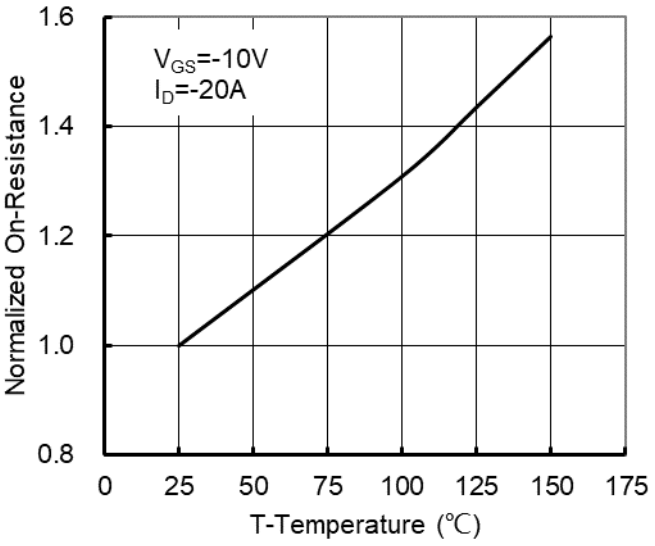


Figure 4: On-Resistance vs. Junction Temperature

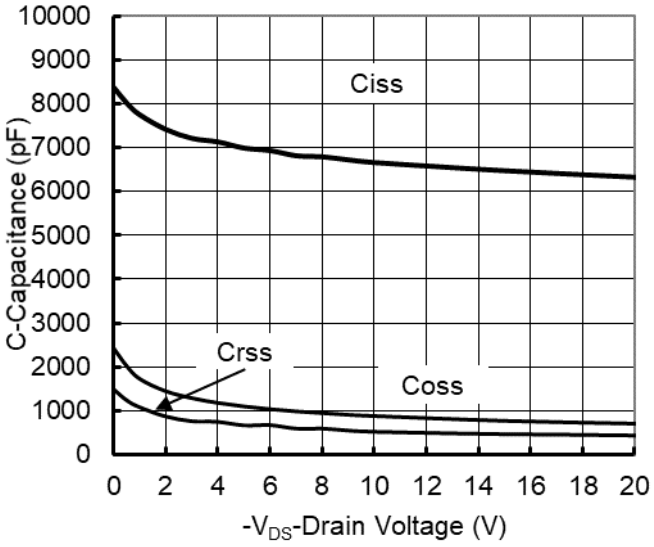


Figure5. Capacitance Characteristics

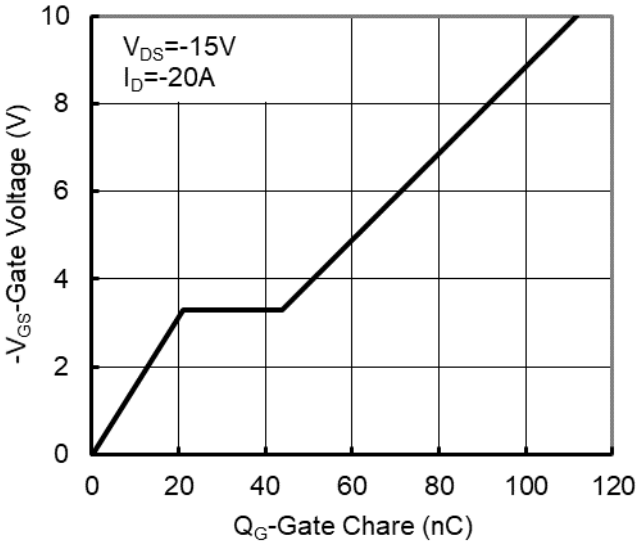


Figure6. Gate Charge

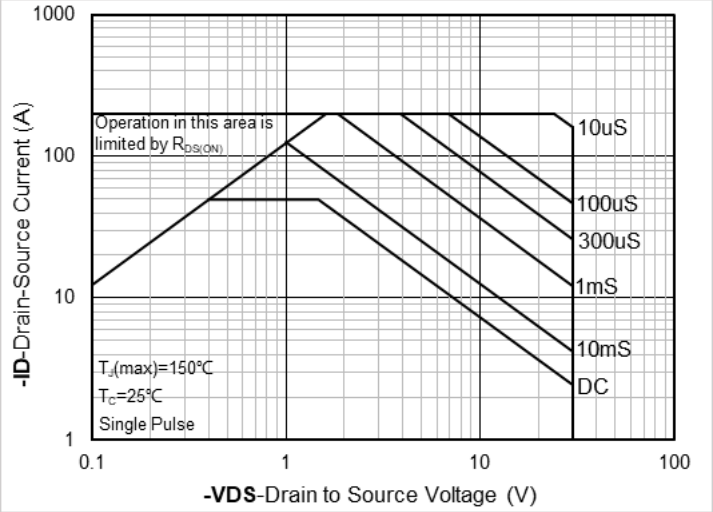


Figure7. Safe Operation Area

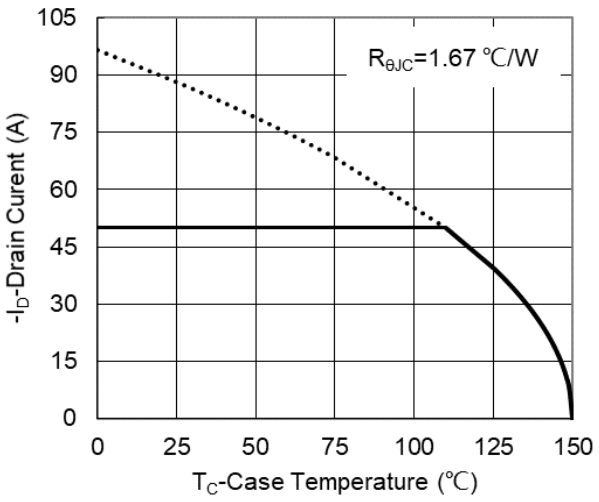


Figure8. Maximum Continuous Drain Current vs Case Temperature

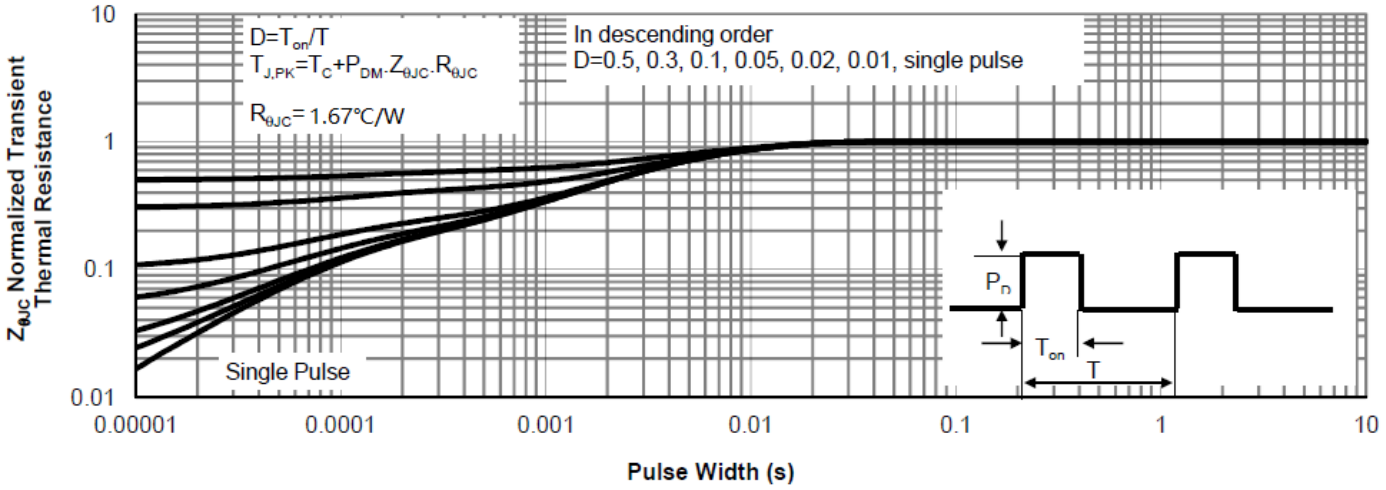
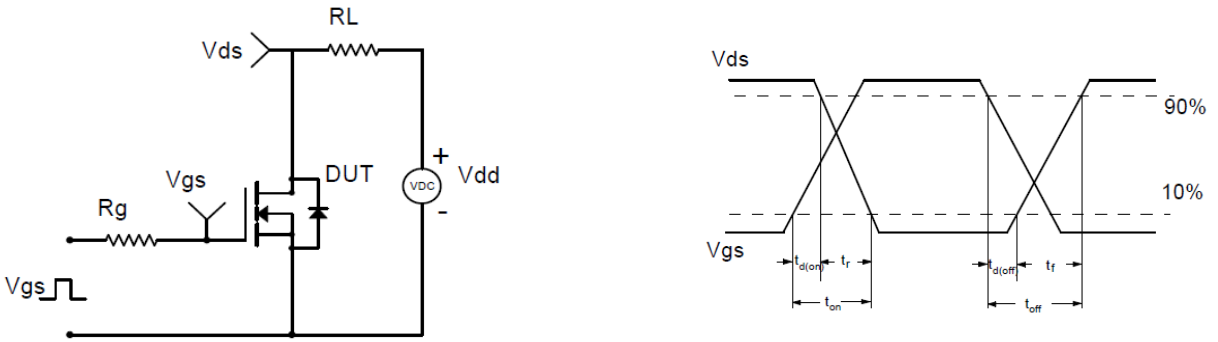
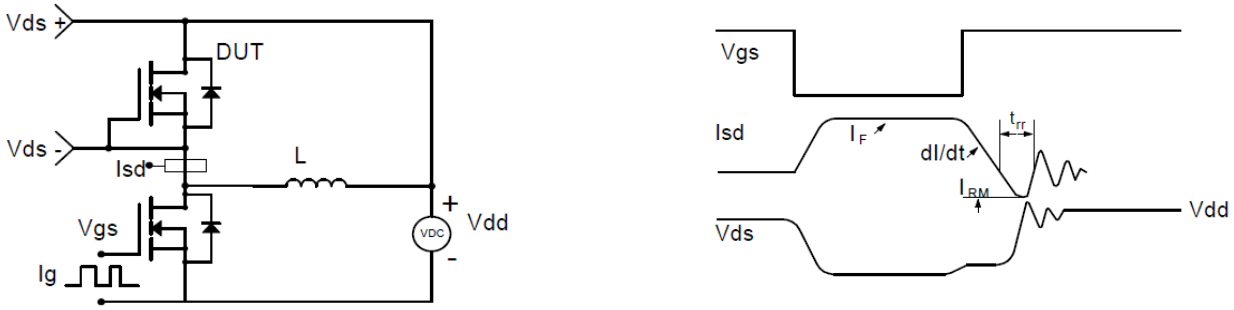


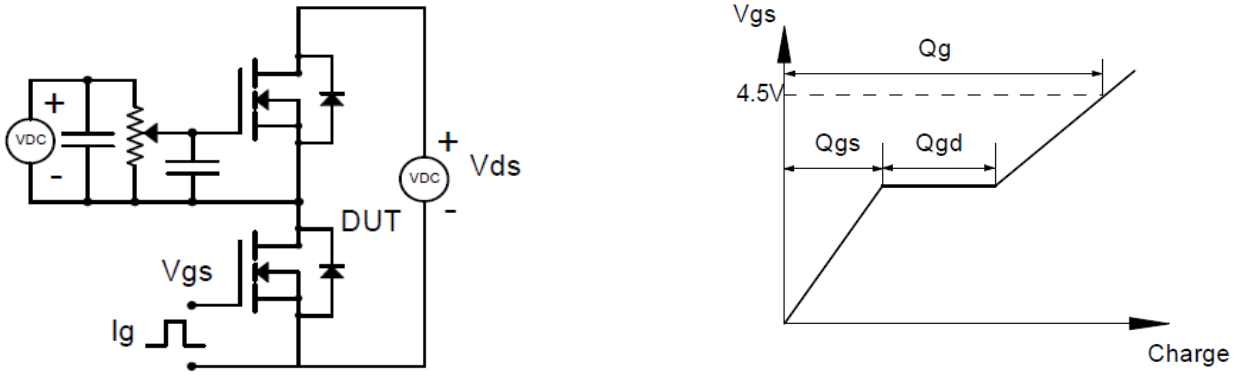
Figure9. Normalized Maximum Transient Thermal Impedance



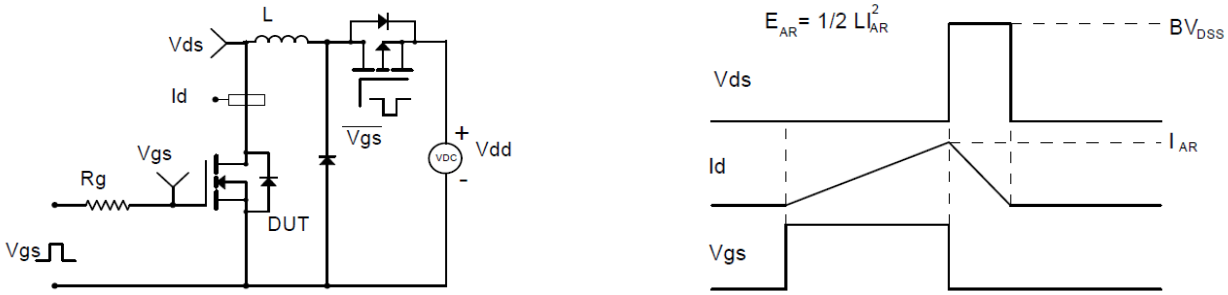
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

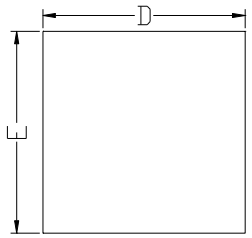


Gate Charge Test Circuit & Waveform

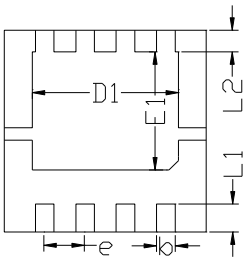


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

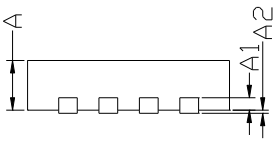
■ DFN3333-8L Package information



Top View
正面视图



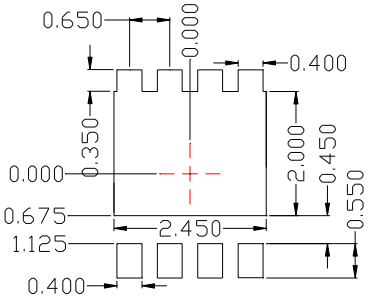
Bottom View
背面视图



Side View
侧面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1		0.20 BSC	
A2			0.10
D1	2.20	2.35	2.50
E1	1.80	1.90	2.00
L1	0.35	0.45	0.55
L2		0.35 BSC	
b	0.20	0.30	0.40
e		0.65 BSC	

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:+/-0.10mm.
3.The pad layout is for reference purposes only.



Suggested Solder Pad Layout
Top View

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