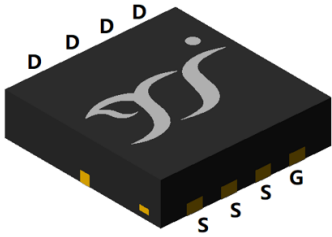
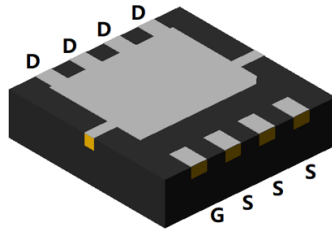


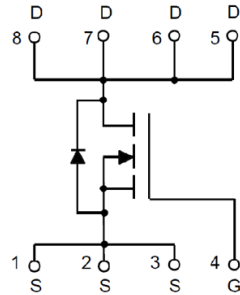
N-Channel Enhancement Mode Field Effect Transistor



Top View



Bottom View



DFN3333-8L

Product Summary

- V_{DS} 30V
- I_D 50A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) <6.0mohm
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) <8.0mohm
- 100% EAS Tested

General Description

- Trench Power LV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 3
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- High current load applications
- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

■ Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	30	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_C=25^\circ C$	I_D	50	A
	$T_C=100^\circ C$		32	
Pulsed Drain Current ^A		I_{DM}	190	A
Total Power Dissipation	$T_C=25^\circ C$	P_D	25	W
	$T_C=100^\circ C$		10	
Single Pulse Avalanche Energy ^B		E_{AS}	112.5	mJ
Thermal Resistance Junction-to-Case ^C		$R_{\theta JC}$	5	$^\circ C/W$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ C$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ50N03B	F1	Q50N03B	5000	10000	100000	13" reel



YJQ50N03B

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1.0	1.5	2.5	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = 10V, I _D =15A		3.9	6.0	mΩ
		V _{GS} = 4.5V, I _D =15A		6.0	8.0	
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V			1.2	V
Maximum Body-Diode Continuous Current	I _S				50	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V, f=1MHZ		2191		pF
Output Capacitance	C _{oss}			300		
Reverse Transfer Capacitance	C _{rss}			247		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =15V, I _D =20A		46.3		nC
Gate-Source Charge	Q _{gs}			8.8		
Gate-Drain Charge	Q _{gd}			9.2		
Reverse Recovery Charge	Q _{rr}	I _F =20A, di/dt=500A/us		1.6		ns
Reverse Recovery Time	t _{rr}			11		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =15V, R _L =0.75Ω R _{GEN} =3Ω		11		ns
Turn-on Rise Time	t _r			80		
Turn-off Delay Time	t _{D(off)}			39		
Turn-off fall Time	t _f			92		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. T_J=25°C, V_{DD}=25V, V_G=10V, L=1mH, I_{AS}=15A

C. R_{θJA} is the sum of the junction-to-Case and Case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design, while R_{θJA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



■ Typical Performance Characteristics

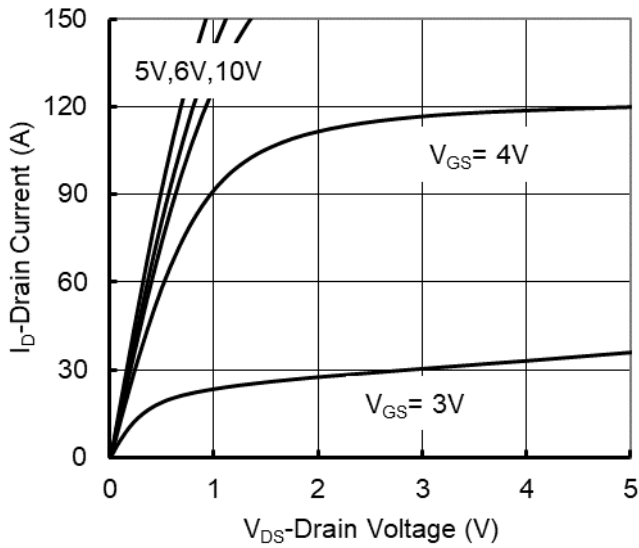


Figure 1. Output Characteristics

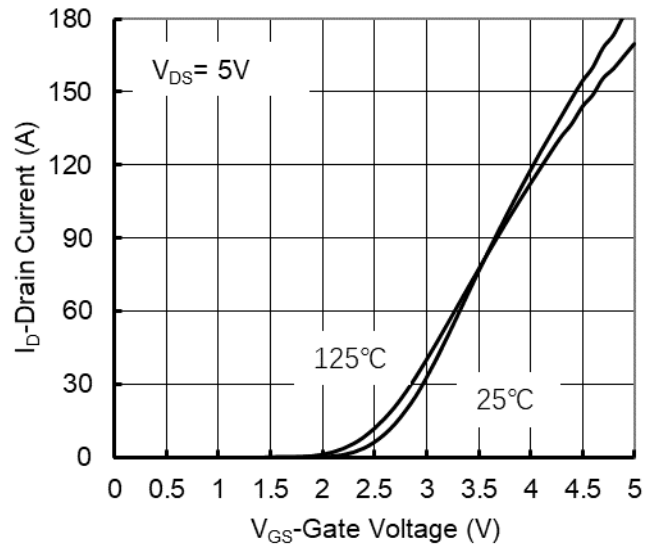


Figure 2. Transfer Characteristics

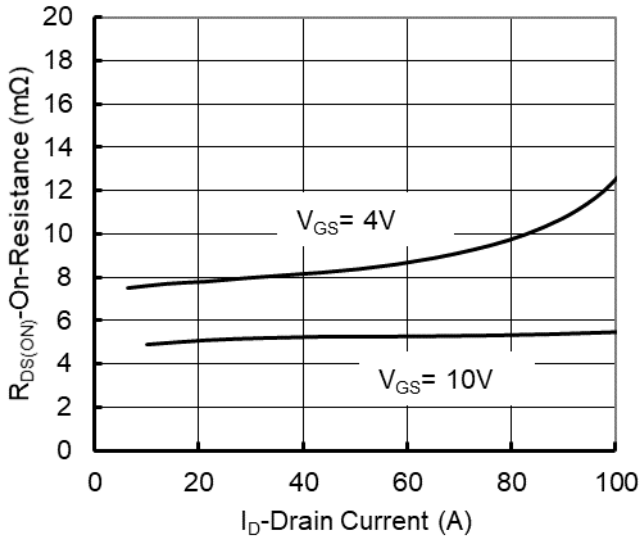


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

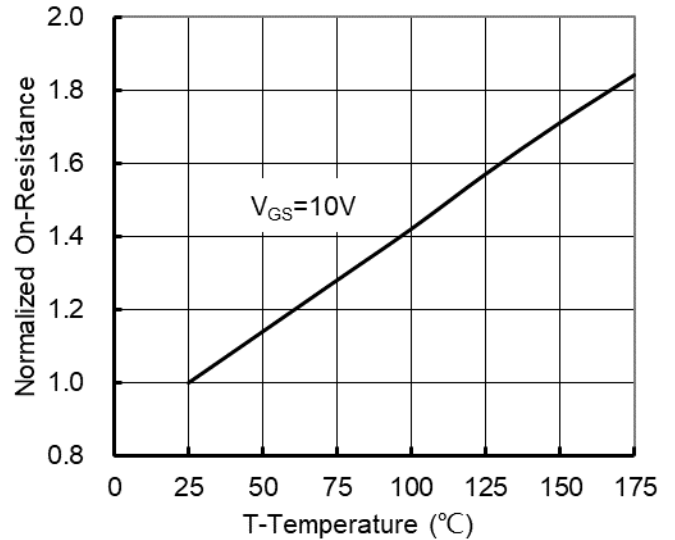


Figure 4. On-Resistance vs. Junction Temperature

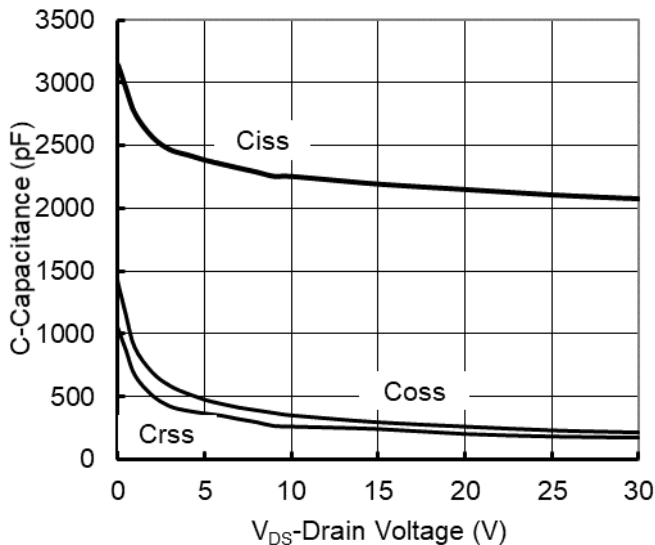


Figure 5. Capacitance Characteristics

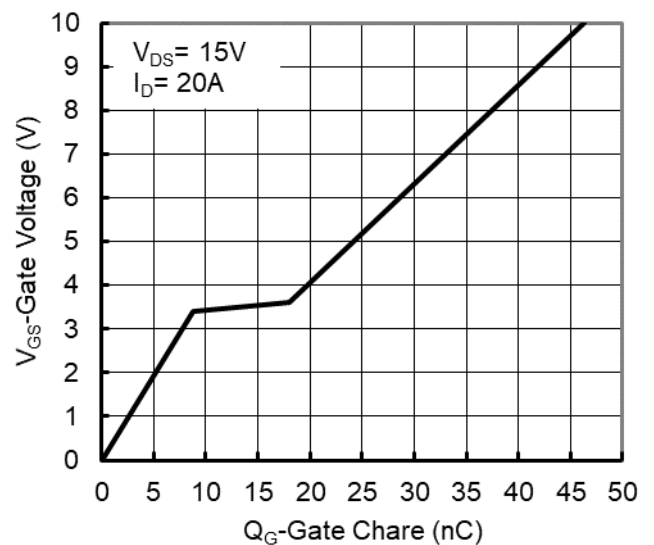


Figure 6. Gate Charge



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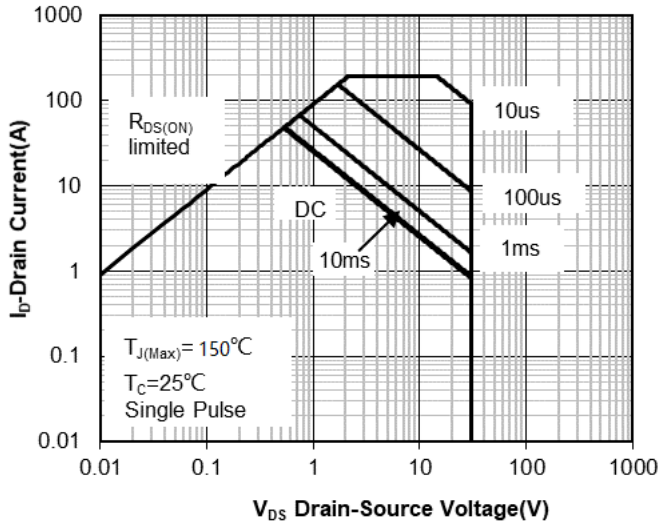


Figure 7. Safe Operation Area

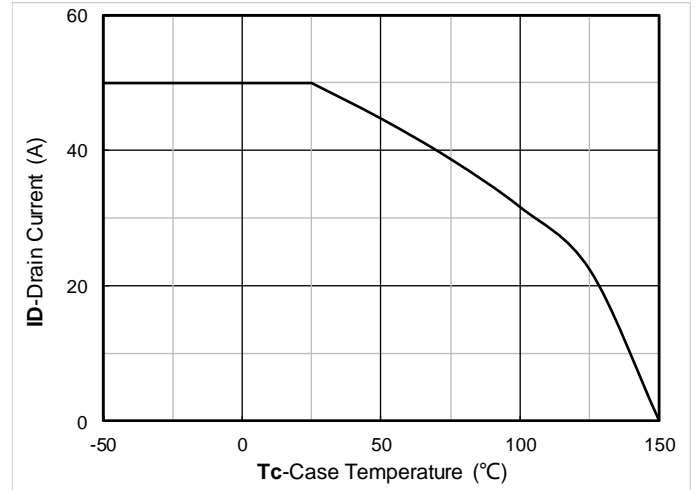


Figure 8. Maximum Continuous Drain Current vs Case Temperature

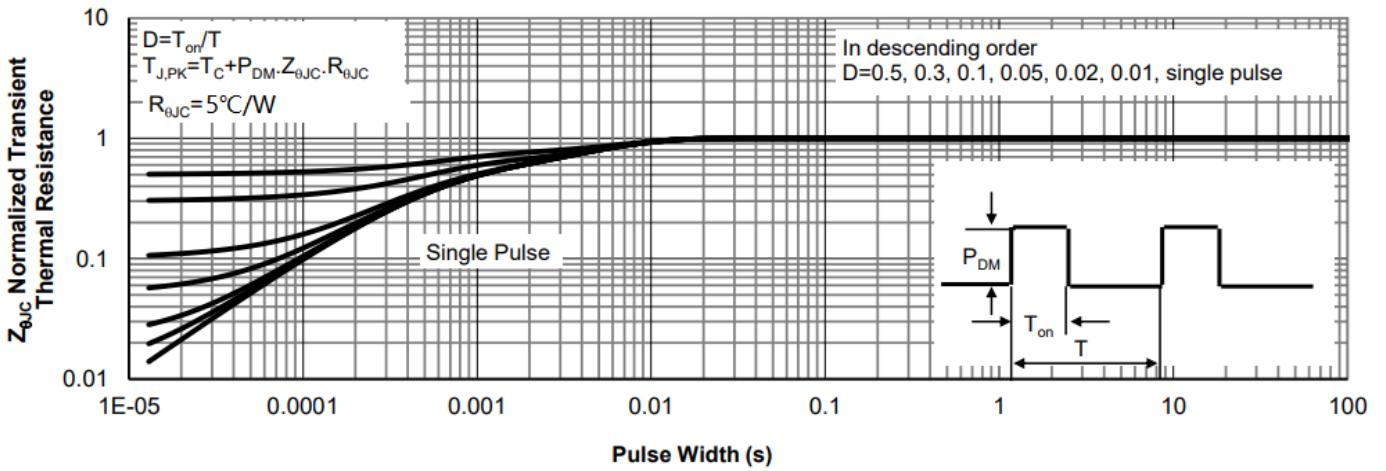
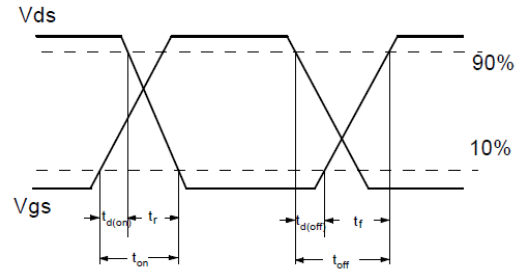
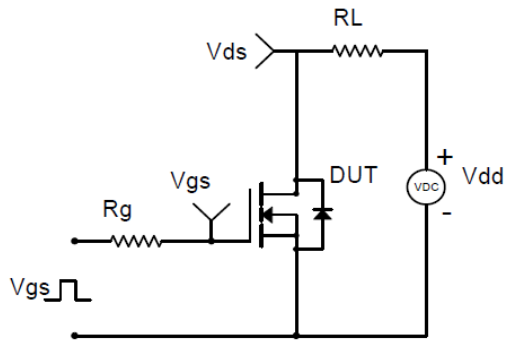
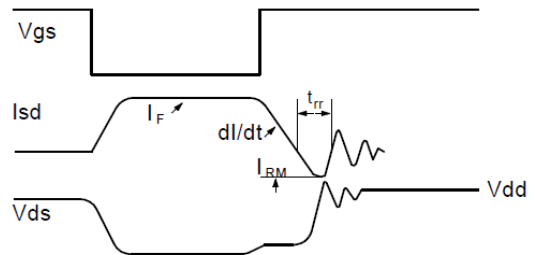
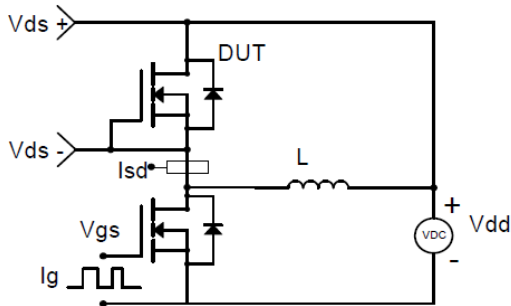


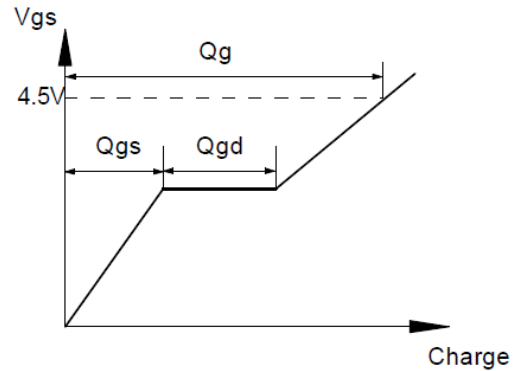
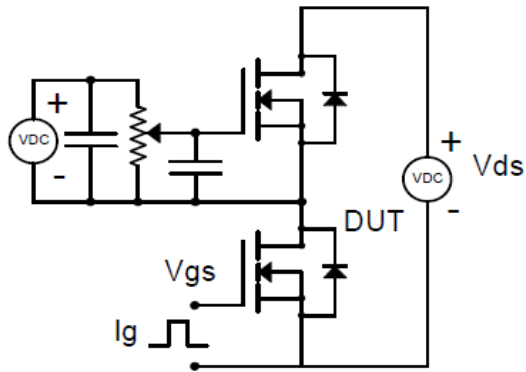
Figure 9. Normalized Maximum Transient Thermal Impedance



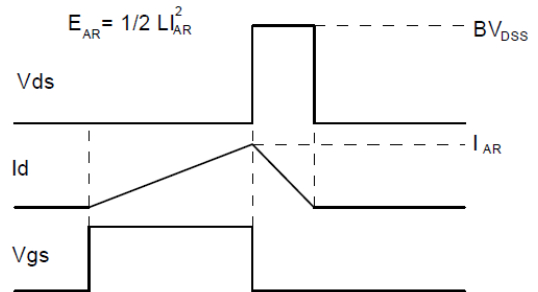
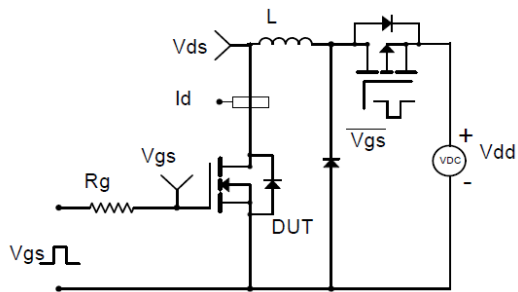
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Gate Charge Test Circuit & Waveform

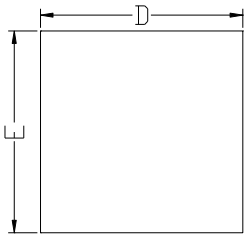


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

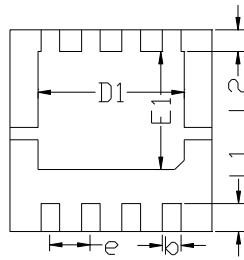


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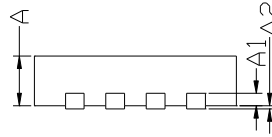
■ DFN3333-8L Package information



Top View
正面视图

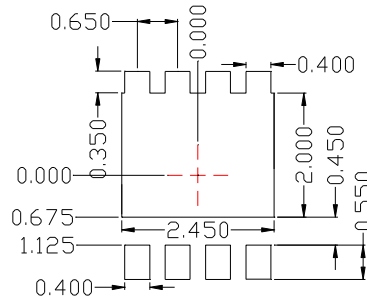


Bottom View
背面视图



Side View
侧面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	2.20	2.35	2.50
E1	1.80	1.90	2.00
L1	0.35	0.45	0.55
L2	0.35 BSC		
k	0.20	0.30	0.40
e	0.65 BSC		



Suggested Solder Pad Layout
Top View

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.10 mm.
3. The pad layout is for reference purposes only.



YJQ50N03B

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