

N-Channel and P-Channel Complementary Power MOSFET

Product Summary

NMOS

• V_{DS}	30V
• I_D	28A
• $R_{DS(ON)}$ (at $V_{GS}=10V$)	< 18mohm
• $R_{DS(ON)}$ (at $V_{GS}=4.5V$)	< 30mohm

PMOS

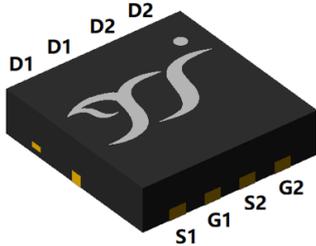
• V_{DS}	-30V
• I_D	-17A
• $R_{DS(ON)}$ (at $V_{GS}=-10V$)	< 45mohm
• $R_{DS(ON)}$ (at $V_{GS}=-4.5V$)	< 65mohm

General Description

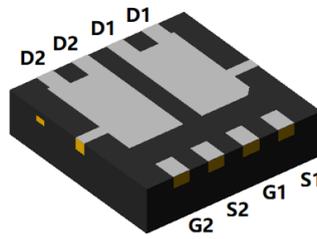
- Trench Power LV MOSFET technology
- High density cell design for low $R_{DS(ON)}$
- High Speed switching
- Moisture Sensitivity Level 3
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Wireless charger
- Load switch
- Power management

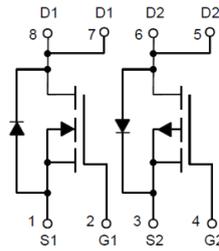


Top View



Bottom View

DFN3333-8L



■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-source Voltage		V_{DS}	30	-30	V
Gate-source Voltage		V_{GS}	± 20	± 20	V
Drain Current	$T_A=25^\circ\text{C}$	I_D	7.5	-5	A
	$T_A=70^\circ\text{C}$		6	-4	
	$T_C=25^\circ\text{C}$		28	-17	
	$T_C=70^\circ\text{C}$		21	-13	
Pulsed Drain Current ^A		I_{DM}	68	-44	A
Total Power Dissipation ^B	$T_A=25^\circ\text{C}$	P_D	2	2	W
	$T_A=70^\circ\text{C}$		1	1	
	$T_C=25^\circ\text{C}$		27	22	
	$T_C=70^\circ\text{C}$		17	14	
Thermal Resistance Junction-to-Ambient ^C		$R_{\theta JA}$	62.5	62.5	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction-to-Case		$R_{\theta JC}$	4.5	5.5	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	-55~+150	$^\circ\text{C}$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ4606A	F1	Q4606	5000	10000	100000	13" reel



YJQ4606A

■ N-MOS Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.0	1.5	2.2	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =14A		15	18	mΩ
		V _{GS} =4.5V, I _D =5A		23	30	
Diode Forward Voltage	V _{SD}	I _S =14A, V _{GS} =0V			1.2	V
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V, f=1MHZ		526		pF
Output Capacitance	C _{oss}			78		
Reverse Transfer Capacitance	C _{rss}			69		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =15V, I _D =5.6A		12.22		nC
Gate-Source Charge	Q _{gs}			2.37		
Gate-Drain Charge	Q _{gd}			2.31		
Reverse Recovery Charge	Q _{rr}	I _F =5.6A, di/dt=100A/us		1.28		ns
Reverse Recovery Time	t _{rr}			16.5		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DS} =15V, I _D =5.6A R _{GEN} =3Ω		5		ns
Turn-on Rise Time	t _r			28.2		
Turn-off Delay Time	t _{D(off)}			12.8		
Turn-off fall Time	t _f			21.6		



YJQ4606A

■ P-MOS Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-30V, V_{GS}=0V$			-1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$			± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.0	-1.5	-2.4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-8A$		36	45	m Ω
		$V_{GS}=-4.5V, I_D=-3.5A$		49	65	
Diode Forward Voltage	V_{SD}	$I_S=-8A, V_{GS}=0V$			-1.2	V
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$		719		pF
Output Capacitance	C_{oss}			78		
Reverse Transfer Capacitance	C_{rss}			64		
Switching Parameters						
Total Gate Charge	Q_g	$V_{GS}=-10V, V_{DS}=-15V, I_D=-5.1A$		14.23		nC
Gate-Source Charge	Q_{gs}			3.16		
Gate-Drain Charge	Q_{gd}			2		
Reverse Recovery Charge	Q_{rr}	$I_F=-5.1A, di/dt=100A/\mu s$		5.3		ns
Reverse Recovery Time	t_{rr}			30		
Turn-on Delay Time	$t_{D(on)}$	$V_{GS}=-10V, V_{DS}=-15V, I_D=5.1A$ $R_{GEN}=3\Omega$		7.4		ns
Turn-on Rise Time	t_r			37		
Turn-off Delay Time	$t_{D(off)}$			31.6		
Turn-off fall Time	t_f			42		

A. Repetitive rating; pulse width limited by max. junction temperature.

B. P_d is based on max. junction temperature, using junction-case thermal resistance.

C. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in2 FR-4 board with 2oz. Copper, in the still air environment with $T_A=25^\circ\text{C}$. The maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design.



■ N-MOS Typical Performance Characteristics

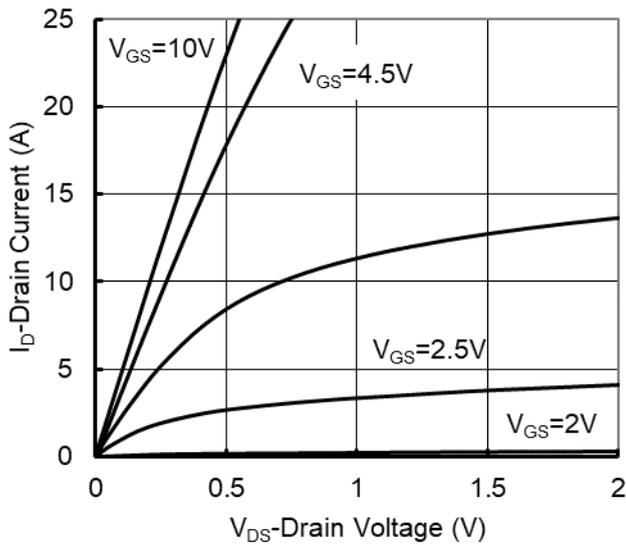


Figure1. Output Characteristics

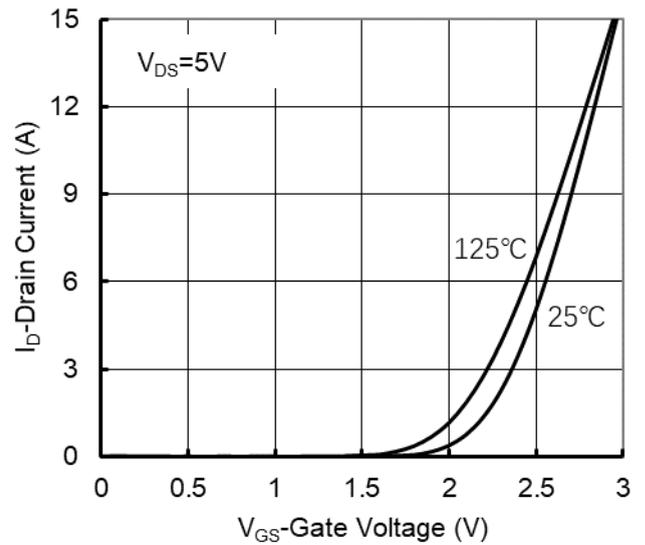


Figure2. Transfer Characteristics

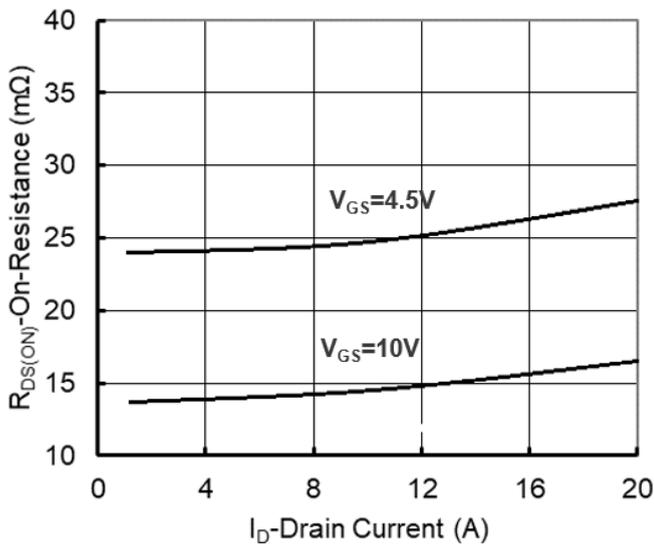


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

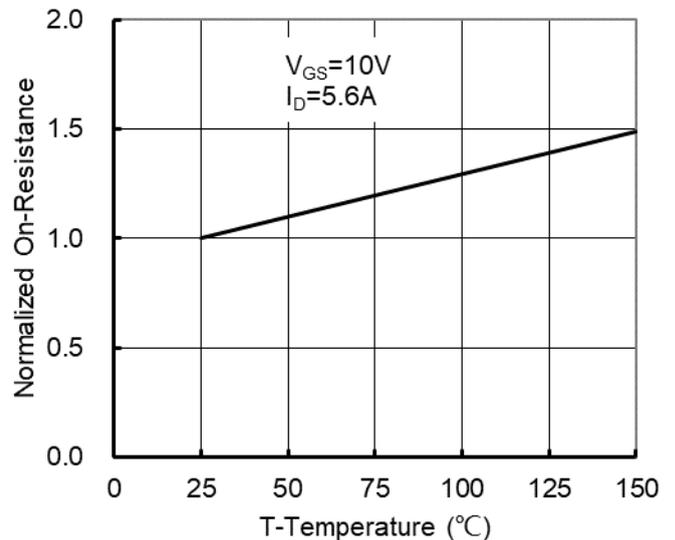


Figure 4: On-Resistance vs. Junction Temperature

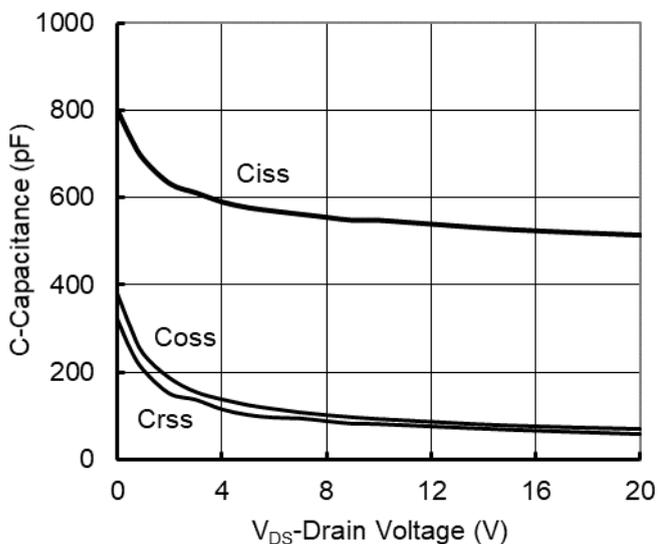


Figure5. Capacitance Characteristics

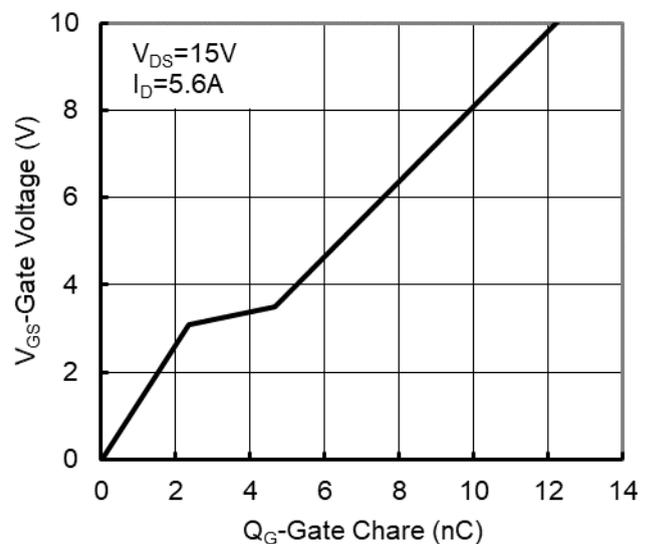


Figure6. Gate Charge



YJQ4606A

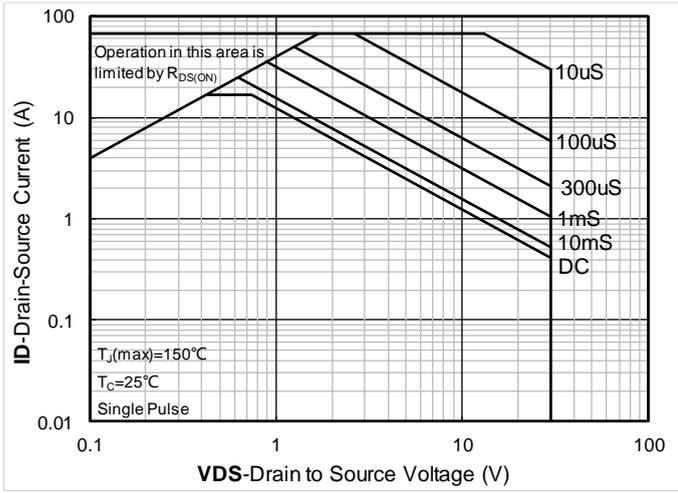


Figure7. Safe Operation Area

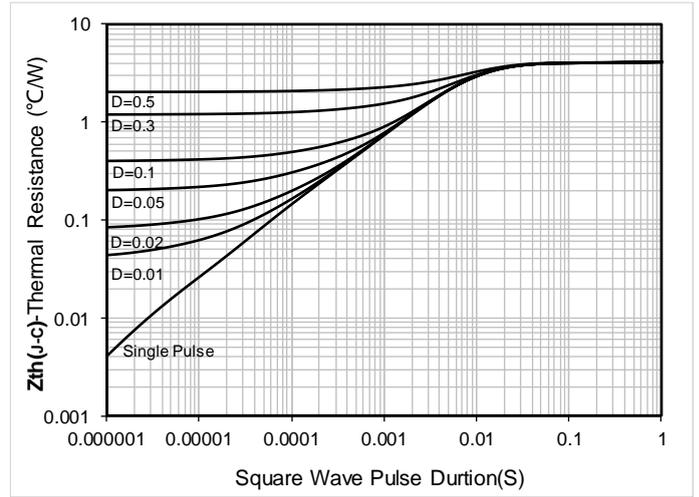


Figure8. Normalized Maximum Transient Thermal Impedance



■ P-MOS Typical Performance Characteristics

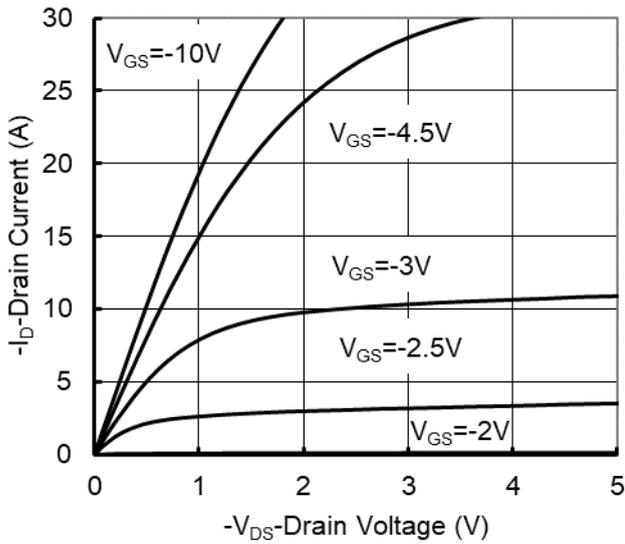


Figure1. Output Characteristics

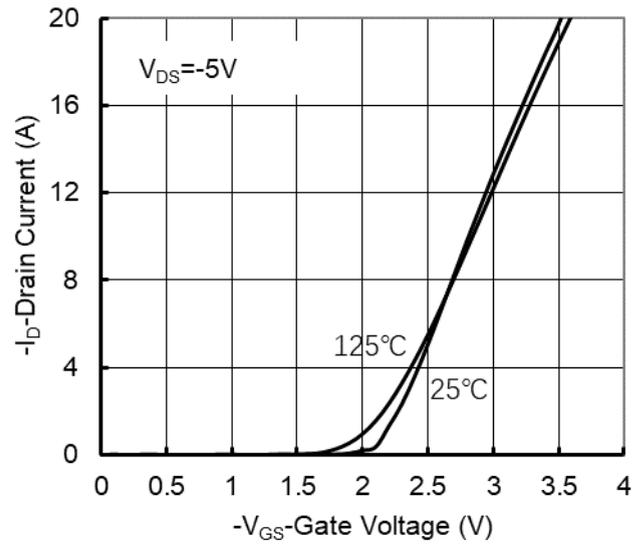


Figure2. Transfer Characteristics

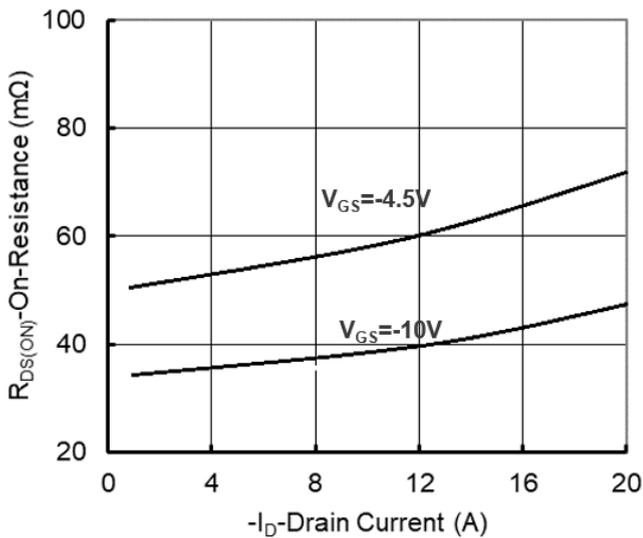


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

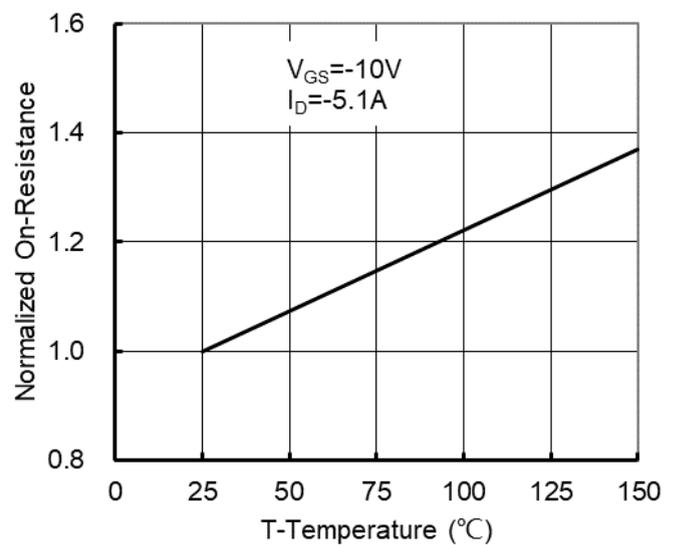


Figure 4: On-Resistance vs. Junction Temperature

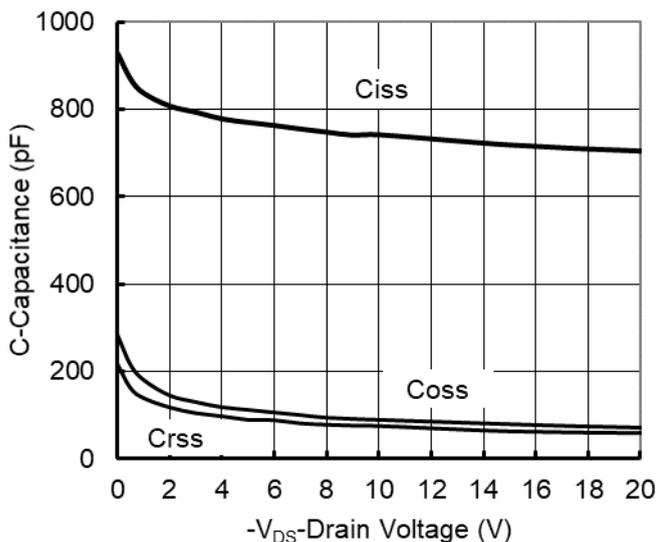


Figure5. Capacitance Characteristics

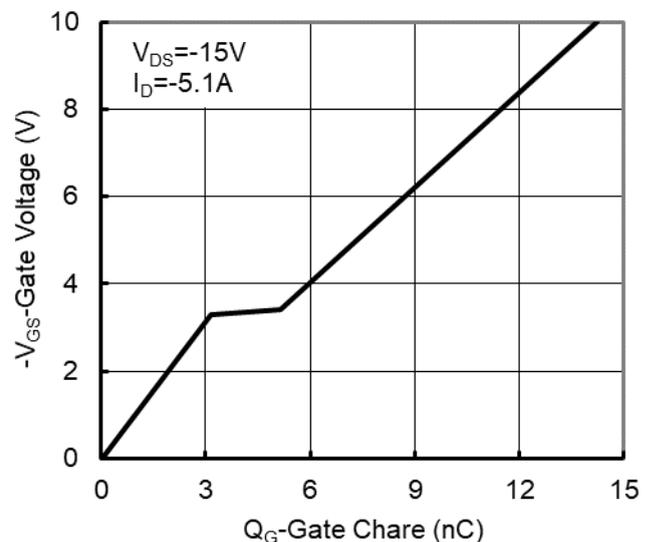


Figure6. Gate Charge



YJQ4606A

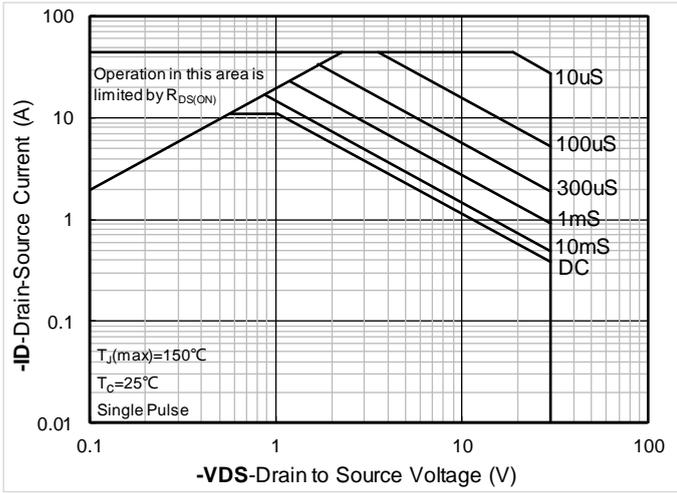


Figure7. Safe Operation Area

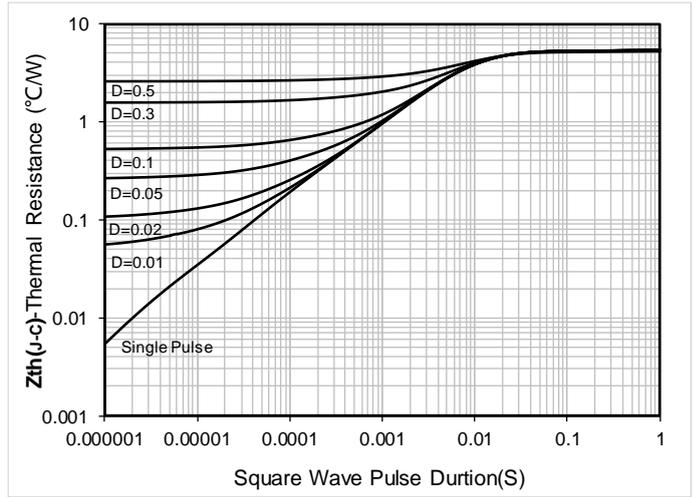
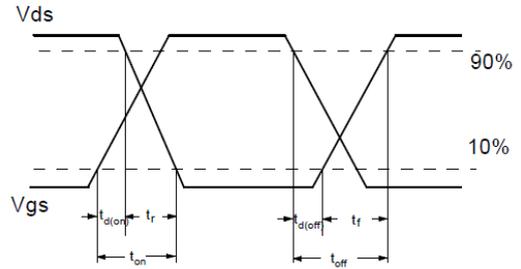
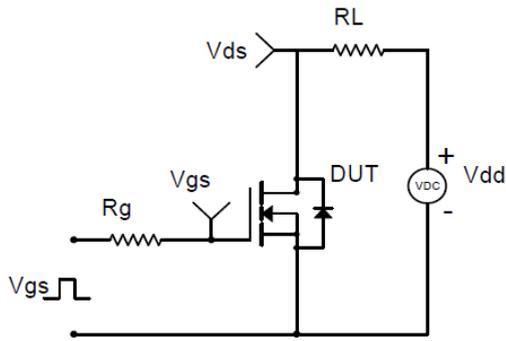
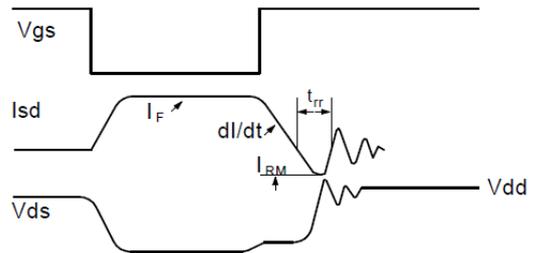
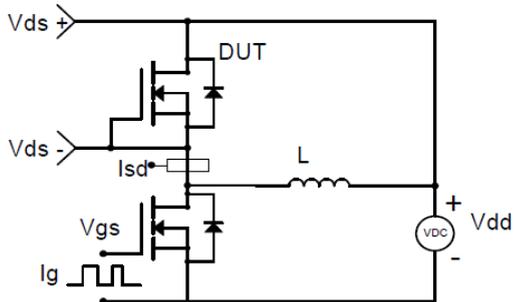


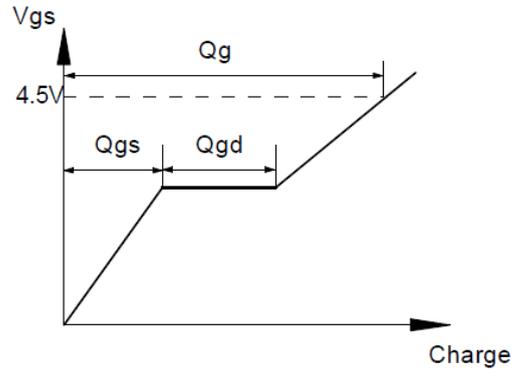
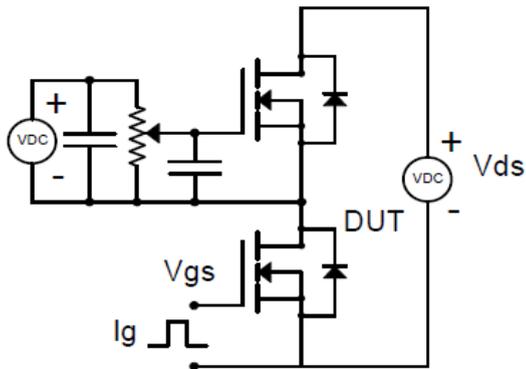
Figure9. Normalized Maximum Transient Thermal Impedance



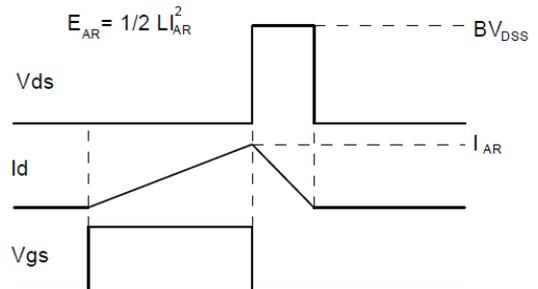
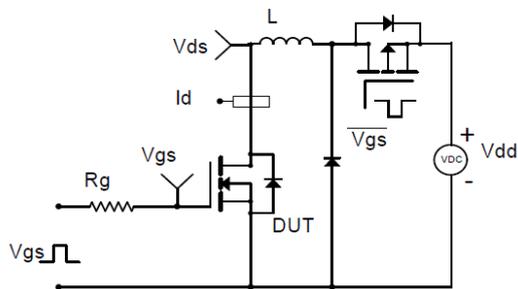
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Gate Charge Test Circuit & Waveform

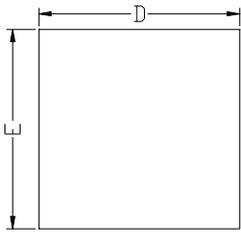


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

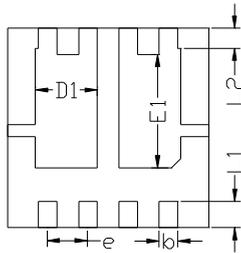


YJQ4606A

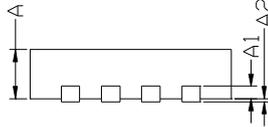
■ DFN3333-8L Package Information



Top View
正面视图

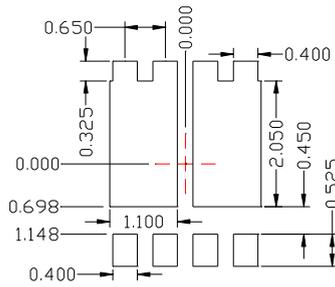


Bottom View
背面视图



Side View
侧面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	0.90	1.00	1.10
E1	1.75	1.85	1.95
L1	0.325	0.425	0.525
L2	0.325 BSC		
b	0.20	0.30	0.40
e	0.65 BSC		



Suggested Solder Pad Layout
Top View

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.10 mm.
3. The pad layout is for reference purposes only.



YJQ4606A

Disclaimer

The information presented in this document is for reference only. Yangzhou Yangjie Electronic Technology Co., Ltd. reserves the right to make changes without notice for the specification of the products displayed herein to improve reliability, function or design or otherwise.

The product listed herein is designed to be used with ordinary electronic equipment or devices, and not designed to be used with equipment or devices which require high level of reliability and the malfunction of which would directly endanger human life (such as medical instruments, transportation equipment, aerospace machinery, nuclear-reactor controllers, fuel controllers and other safety devices), Yangjie or anyone on its behalf, assumes no responsibility or liability for any damages resulting from such improper use of sale.

This publication supersedes & replaces all information previously supplied. For additional information, please visit our website [http:// www.21yangjie.com](http://www.21yangjie.com) , or consult your nearest Yangjie's sales office for further assistance.