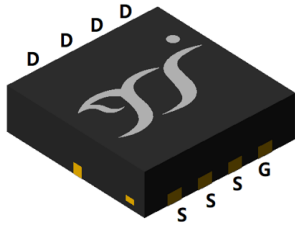
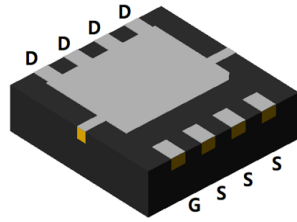


P-Channel Enhancement Mode Field Effect Transistor

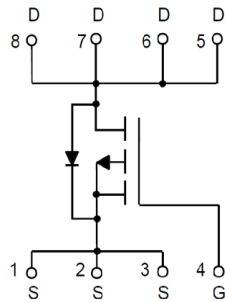


Top View



Bottom View

DFN3333-8L



Product Summary

- V_{DS} -30V
- I_D -40A
- $R_{DS(ON)}$ (at $V_{GS}=-20V$) <13mohm
- $R_{DS(ON)}$ (at $V_{GS}=-10V$) <15mohm
- $R_{DS(ON)}$ (at $V_{GS}=-4.5V$) <25mohm
- 100% EAS Tested

General Description

- Trench Power LV MOSFET technology
- High density cell design for Low $R_{DS(ON)}$
- High Speed switching
- Moisture Sensitivity Level 3
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Battery protection
- Power management
- Load switch

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Maximum	Unit
Drain-source Voltage	V_{DS}	-30	V
Gate-source Voltage	V_{GS}	± 25	V
Drain Current	I_D	$T_A=25^\circ\text{C}$	-14
		$T_A=100^\circ\text{C}$	-9
		$T_C=25^\circ\text{C}$	-40
		$T_C=100^\circ\text{C}$	-25
Pulsed Drain Current ^A	I_{DM}	-160	A
Single Pulse Avalanche Energy @ $L=0.5\text{mH}$ ^B	E_{AS}	72	mJ
Total Power Dissipation ^C	P_D	$T_A=25^\circ\text{C}$	2.5
		$T_A=100^\circ\text{C}$	1
		$T_C=25^\circ\text{C}$	32
		$T_C=100^\circ\text{C}$	12.5
Thermal Resistance Junction-to-Case @ Steady State ^D	$R_{\theta JC}$	4.0	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction-to-Ambient @ Steady State ^D	$R_{\theta JA}$	50	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	T_J, T_{STG}	-55~+150	$^\circ\text{C}$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ40P03A	F1	Q40P03	5000	10000	100000	13" reel



YJQ40P03A

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250μA	-30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-30V, V _{GS} =0V, T _C =25°C			-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±25V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =-250μA	-1.2	-1.8	-2.8	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = -20V, I _D =-20A		8.6	13	mΩ
		V _{GS} = -10V, I _D =-15A		9.8	15	
		V _{GS} = -6.0V, I _D =-12A		12.1	22	
		V _{GS} = -4.5V, I _D =-10A		15.5	25	
Diode Forward Voltage	V _{SD}	I _S =-20A, V _{GS} =0V			-1.2	V
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =-15V, V _{GS} =0V, f=1MHZ		2152		pF
Output Capacitance	C _{oss}			308		
Reverse Transfer Capacitance	C _{rss}			242		
Gate Resistance	R _g	f= 1MHZ			20	Ω
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =-10V, V _{DS} =-15V, I _D =-12A		40.1		nC
Gate Source Charge	Q _{gs}			8.4		
Gate Drain Charge	Q _{gd}			8.6		
Reverse Recovery Charge	Q _{rr}	I _F = -12A, di/dt=100A/us		7.8		ns
Reverse Recovery Time	t _{rr}			18		
Turn-on Delay Time	t _{D(on)}	V _{GS} =-10V, V _{DD} =-15V, I _D =-1A, R _{GEN} =2.5Ω		8		ns
Turn-on Rise Time	t _r			19		
Turn-off Delay Time	t _{D(off)}			75		
Turn-off Fall Time	t _f			46		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. T_J=25°C, V_{DD}=-30V, V_G=-10V, R_G=25Ω, L=1mH, I_{AS}=-15A.

C. P_d is based on max. junction temperature, using junction-case thermal resistance.

D. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design, while R_{θJA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



■ Typical Performance Characteristics

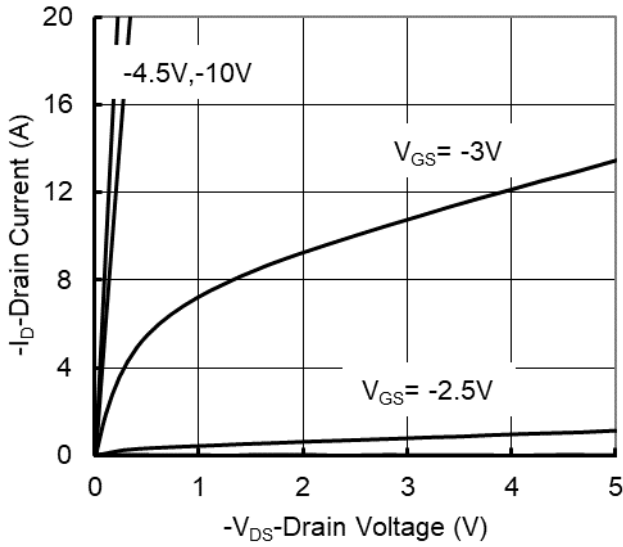


Figure 1. Output Characteristics

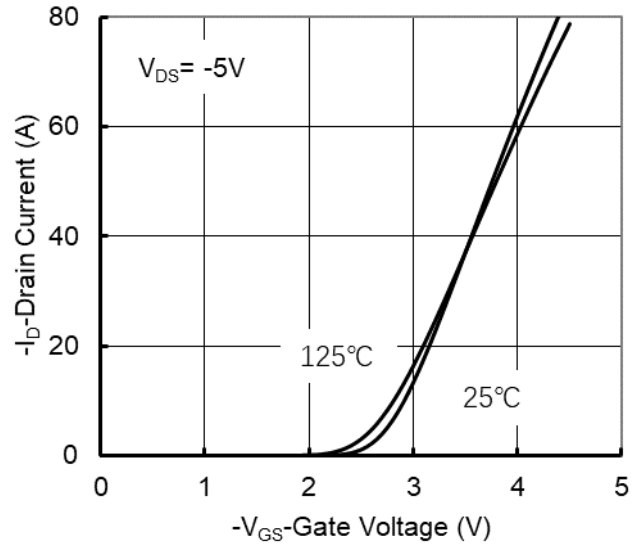


Figure 2. Transfer Characteristics

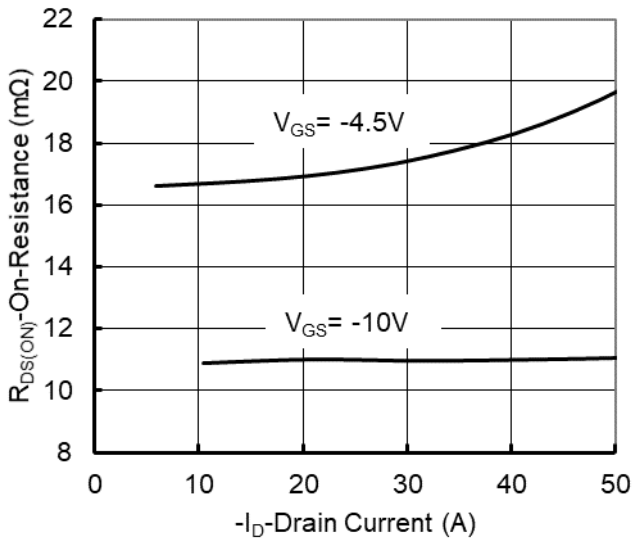


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

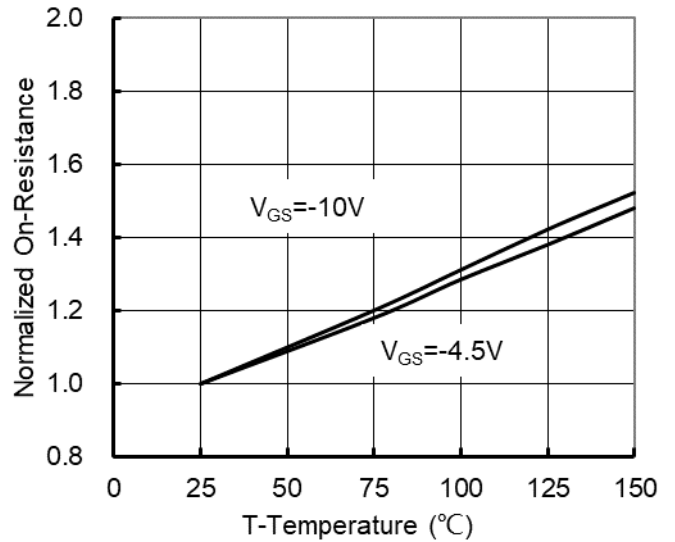


Figure 4. On-Resistance vs. Junction Temperature

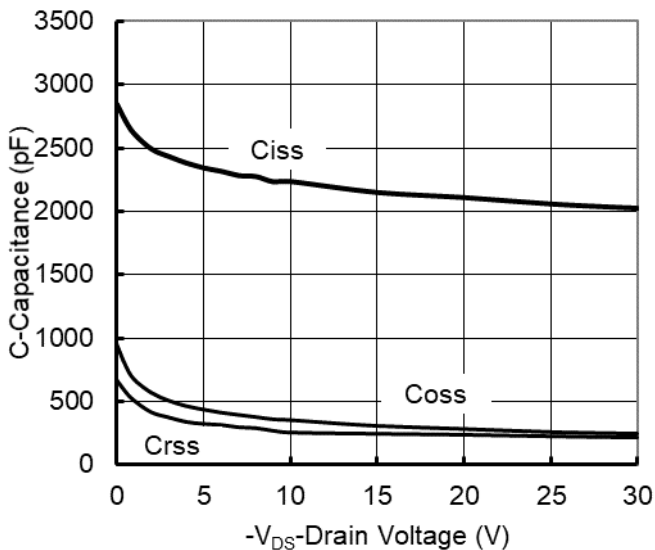


Figure 5. Capacitance Characteristics

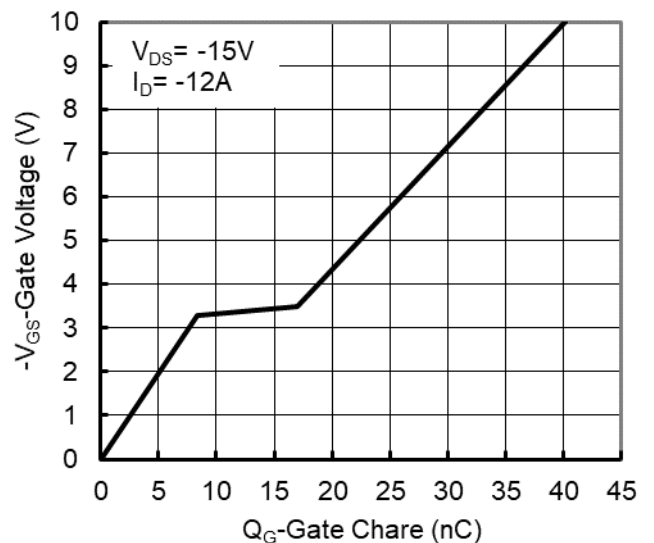


Figure 6. Gate Charge



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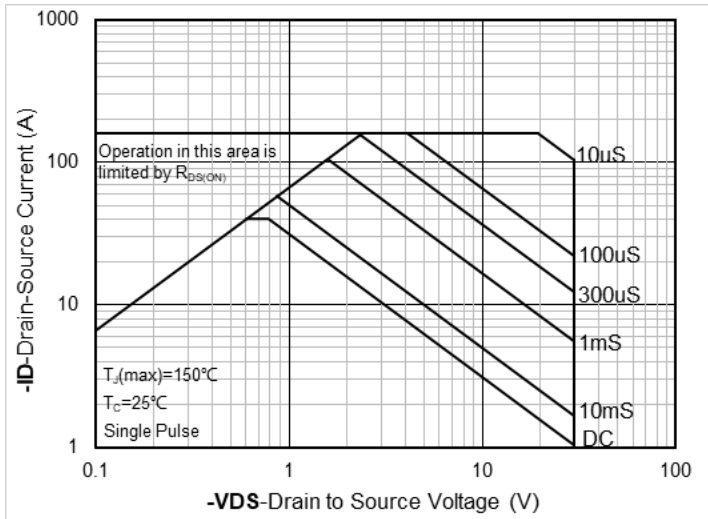


Figure 7. Safe Operation Area

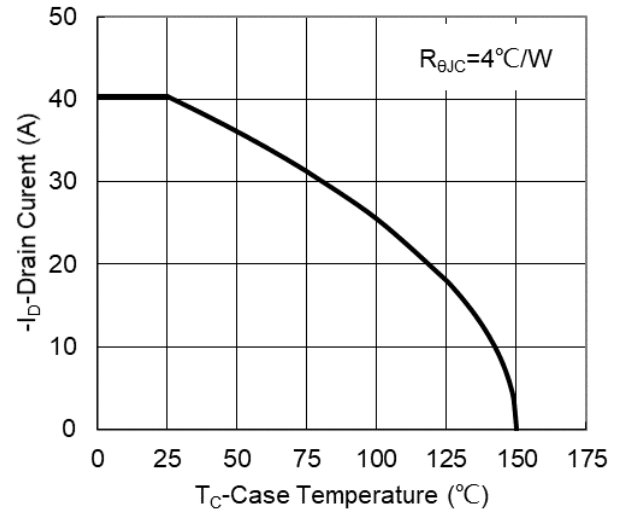


Figure 8. Maximum Continuous Drain Current vs Case Temperature

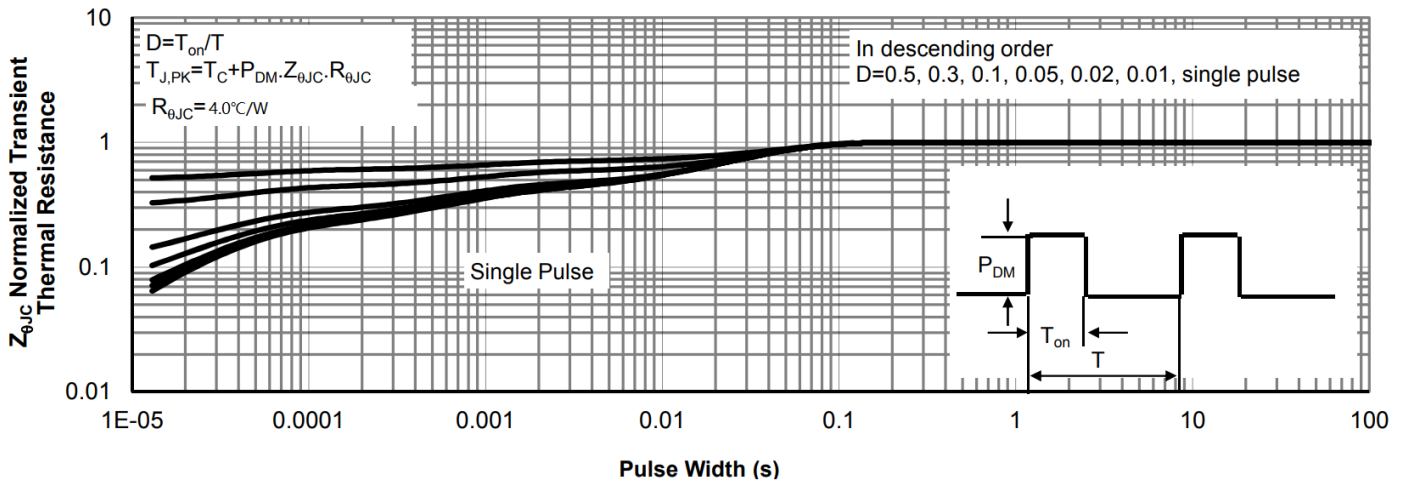
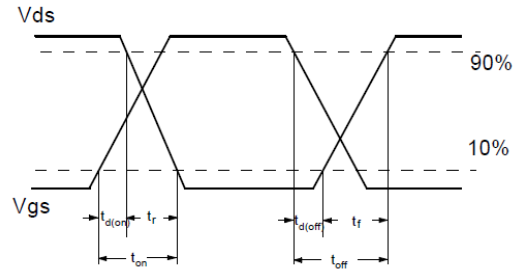
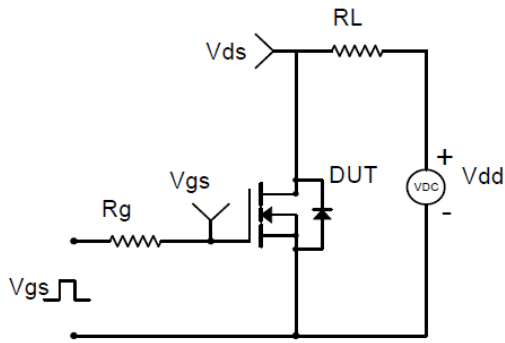
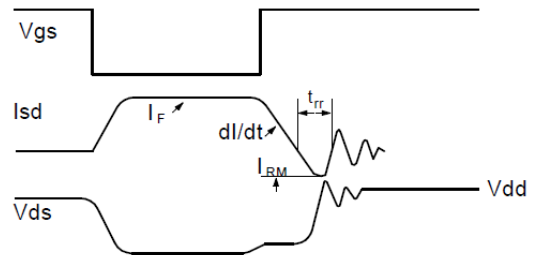
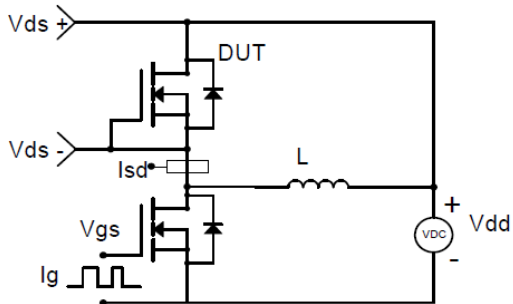


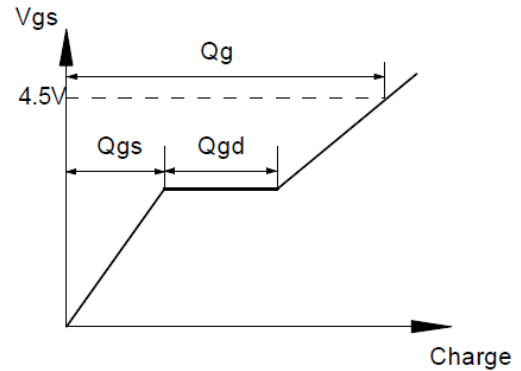
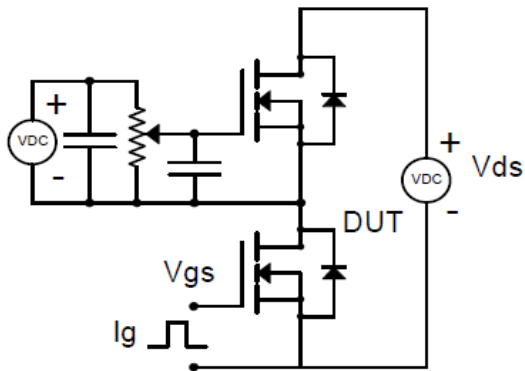
Figure 9. Normalized Maximum Transient Thermal Impedance



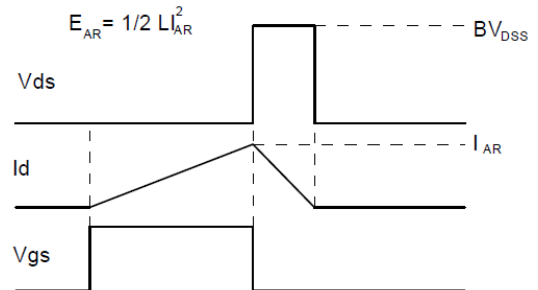
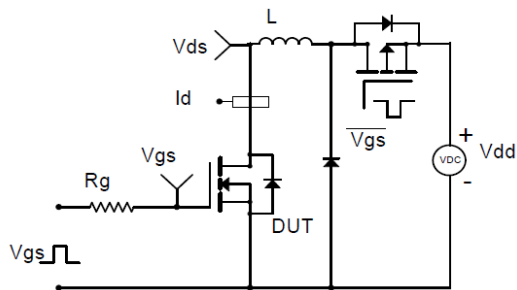
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Gate Charge Test Circuit & Waveform

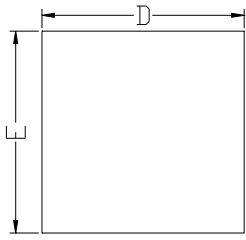


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

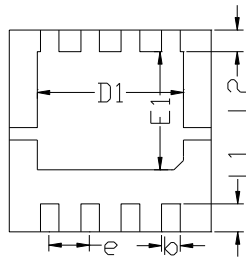


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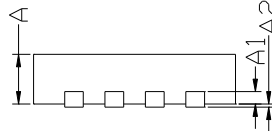
DFN3333-8L Package Information



Top View
正面视图

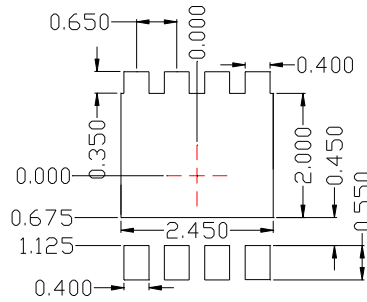


Bottom View
背面视图



Side View
侧面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	2.20	2.35	2.50
E1	1.80	1.90	2.00
L1	0.35	0.45	0.55
L2	0.35 BSC		
b	0.20	0.30	0.40
e	0.65 BSC		



Suggested Solder Pad Layout
Top View

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.10 mm.
3. The pad layout is for reference purposes only.



YJQ40P03A

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