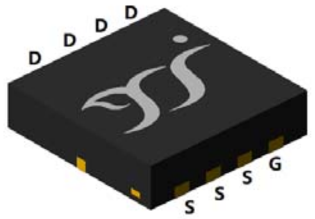
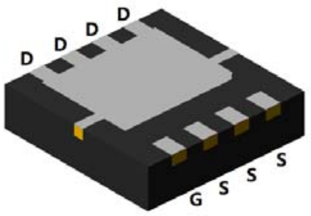
P-Channel Enhancement Mode Field Effect Transistor

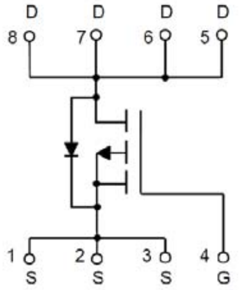


Top View



Bottom View

DFN3333-8L



Product Summary

● V_{DS}	-100V
● I_D	-15A
● $R_{DS(ON)}$(at V_{GS}=10V)	＜110mΩ
● $R_{DS(ON)}$(at V_{GS}=4.5V)	＜120mΩ
● 100% EAS Tested	

General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Part no. with suffix ”Q” means AEC-Q101 qualified

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor
- 12V, 24V and 48V Automotive systems

■ Absolute Maximum Ratings (T_A=25℃ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	-100	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current	T_A=25℃	I_D	-3.9	A
	T_A=100℃		-2.5	
	T_C=25℃		-15	
	T_C =100℃		-9.5	
Pulsed Drain Current [A]		I_{DM}	-35	A
Avalanche energy [B]		EAS	64	mJ
Total Power Dissipation [C]	T_A=25℃	P_D	2.5	W
	T_A=100℃		1	
	T_C=25℃		43	
	T_C =100℃		17.2	
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

■Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient [D]	Steady-State	$R_{\theta JA}$	40	50	℃/W
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	2.4	2.9	

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ15GP10AQ	F1	Q15GP10A	5000	10000	100000	13“ reel

■ **Electrical Characteristics** (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=-250μA	-100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-100V, V_{GS}=0V			-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250μA	-1.0	-1.8	-2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= -10V, I_D=-10A		83	110	mΩ
		V_{GS}= -4.5V, I_D=-5A		95	120	
Diode Forward Voltage	V_{SD}	I_S=-15A,V_{GS}=0V	-		-1.3	V
Maximum Body-Diode Continuous Current	I_S		-	-	-15	A
Dynamic Parameters						
Gate resistance	R_G	f=1MHz, Open drain	-	10	-	Ω
Input Capacitance	C_{iss}	V_{DS}=-25V, V_{GS}=0V, f=1MHz	-	1200	-	pF
Output Capacitance	C_{oss}		-	200	-	
Reverse Transfer Capacitance	C_{rss}		-	25	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=-10V,V_{DS}=-50V,I_D=-5A		20.1	-	nC
Gate-Source Charge	Q_{gs}		-	3.98	-	
Gate-Drain Charge	Q_{gd}		-	4.38	-	
Reverse Recovery Charge	Q_{rr}	I_F=-5A, di/dt=100A/us	-	140	-	nC
Reverse Recovery Time	t_{rr}		-	80	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-10V,V_{DD}=-50V,I_{DS}=-5A R_{GEN}=6Ω	-	10	-	ns
Turn-on Rise Time	t_r		-	30	-	
Turn-off Delay Time	$t_{D(off)}$		-	77	-	
Turn-off fall Time	t_f		-	81	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B. TJ=25℃, V_{DD}=-50V, V_G=-10V, R_G=25Ω, L=0.5mH, IAS=-16A.

C. Pd is based on max. junction temperature, using junction-case thermal resistance.

D. The value of RθJA is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with TA =25° C. The Power dissipation PDSM is based on RθJA t≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

■Typical Electrical and Thermal Characteristics Diagrams

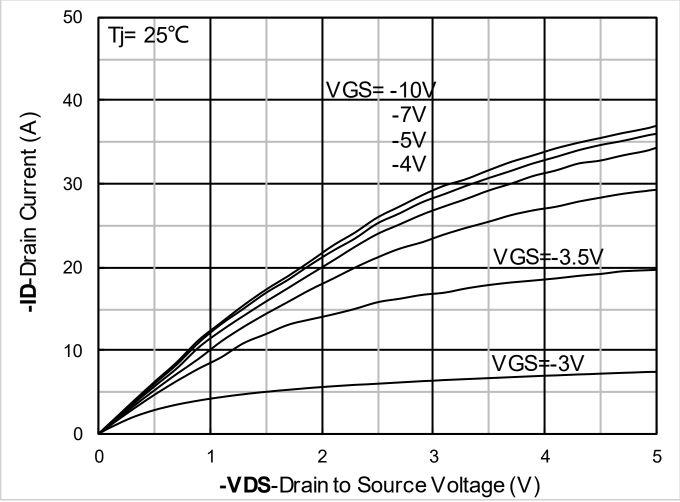


Figure 1. Output Characteristics

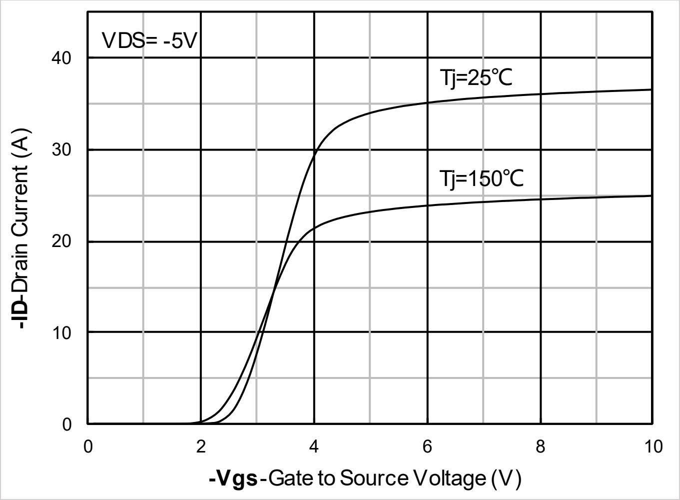


Figure 2. Transfer Characteristics

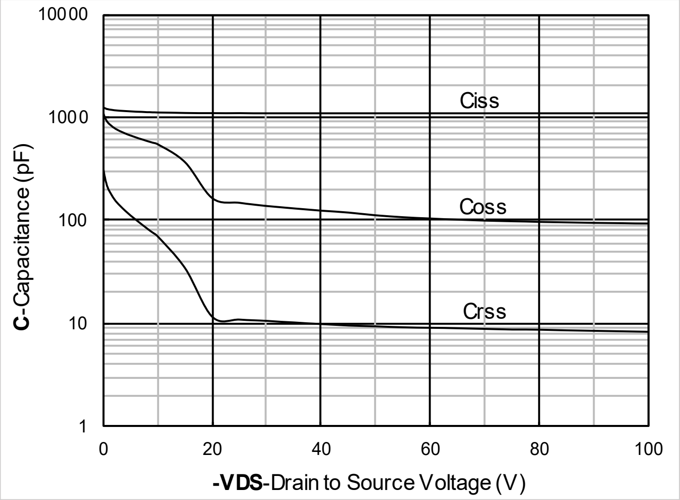


Figure 3. Capacitance Characteristics

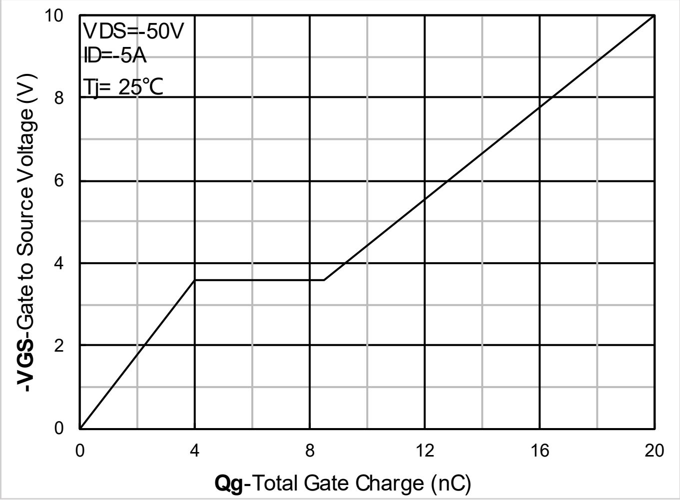


Figure 4. Gate Charge

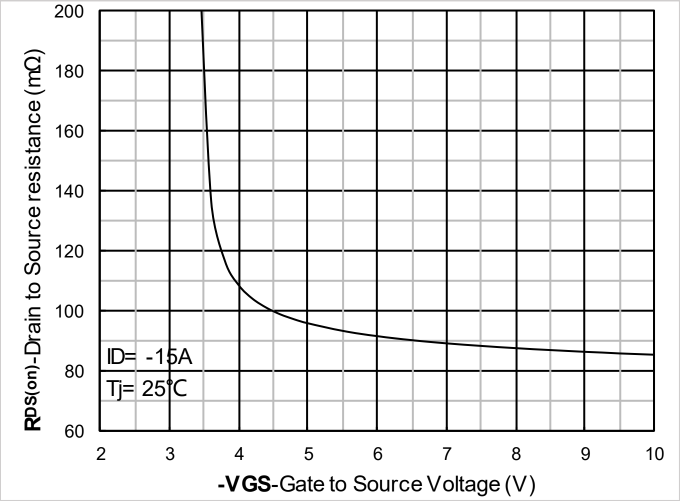


Figure 5. On-Resistance vs Gate to Source Voltage

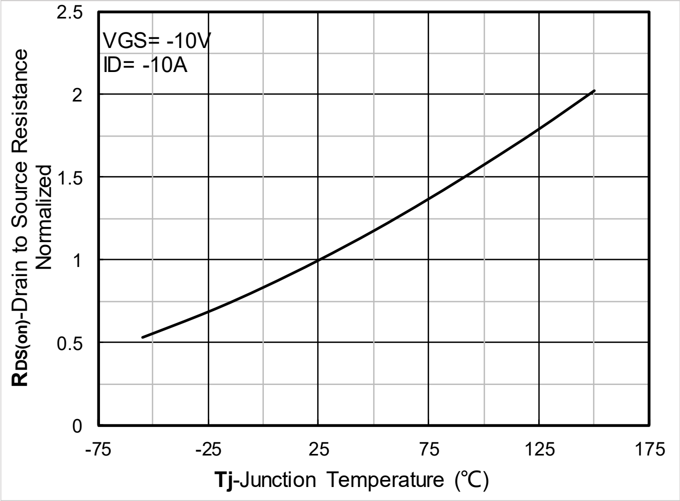


Figure 6. Normalized On-Resistance

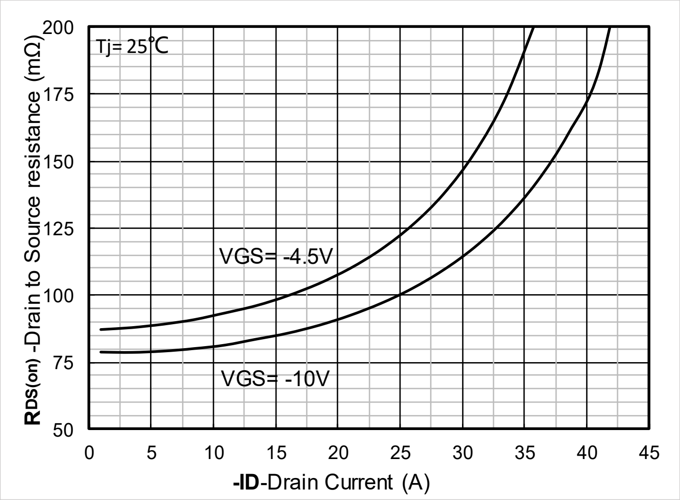


Figure 7. RDS(on) VS Drain Current

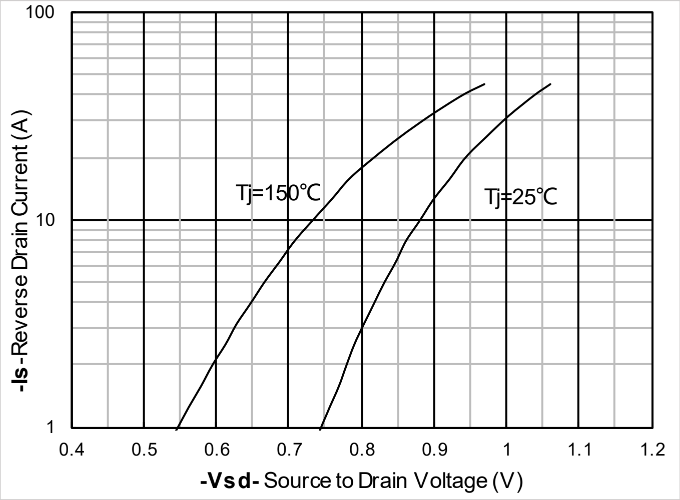


Figure 8. Forward characteristics of reverse diode

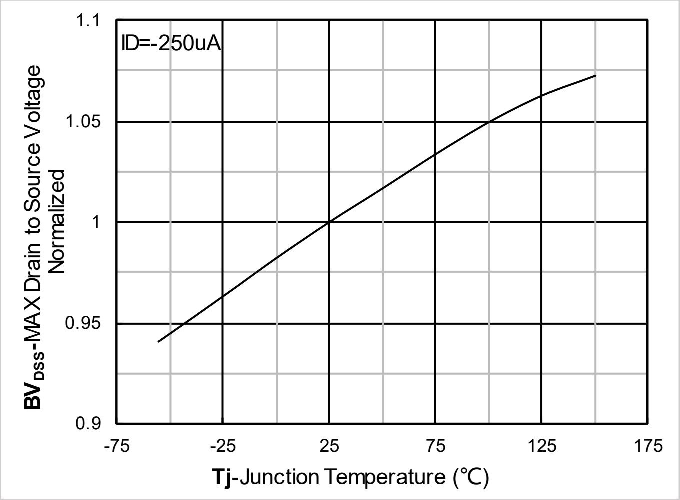


Figure 9. Normalized breakdown voltage

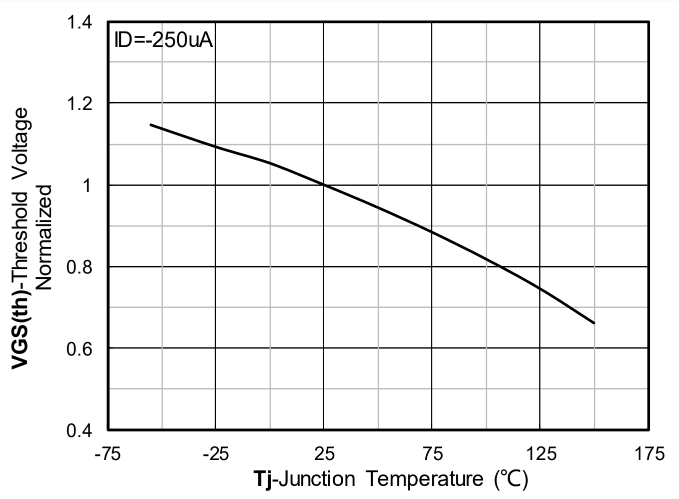


Figure 10. Normalized Threshold voltage

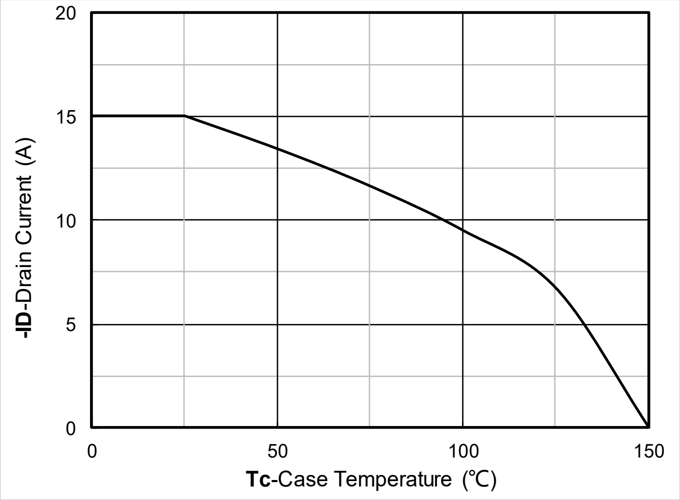


Figure 11. Current dissipation

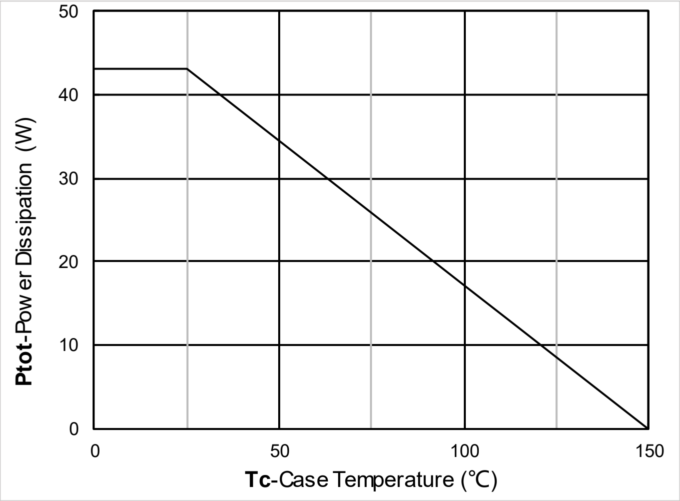


Figure 12. Power dissipation

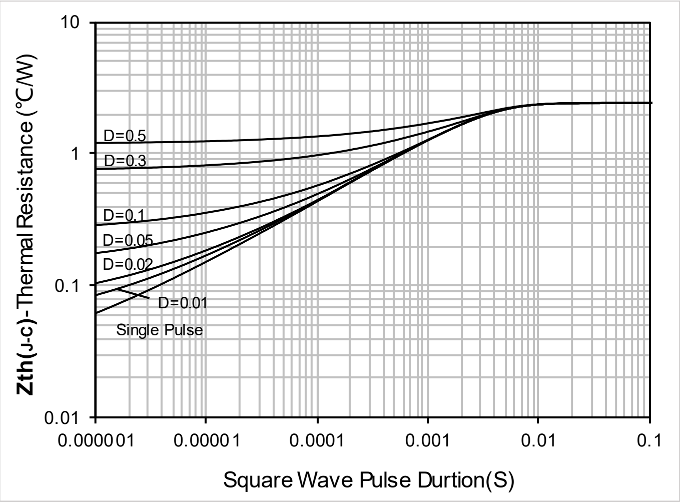


Figure 13. Maximum Transient Thermal Impedance

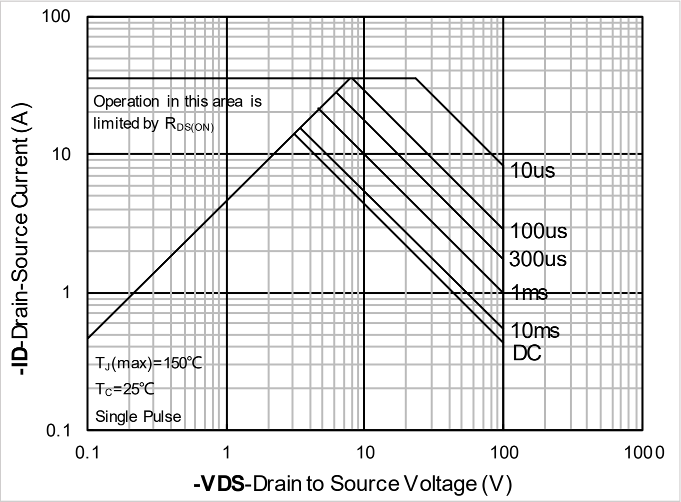
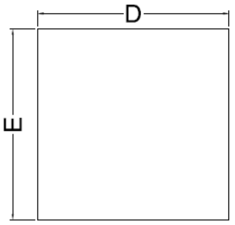
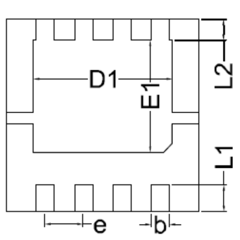


Figure 14. Safe Operation Area

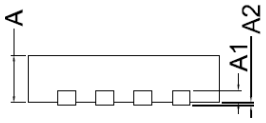
■DFN3333-8L Package information



Top View
正面视图

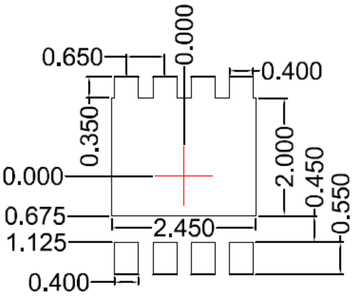


Bottom View
背面视图



Side View
侧面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	2.20	2.35	2.50
E1	1.80	1.90	2.00
L1	0.35	0.45	0.55
L2	0.35 BSC		
b	0.20	0.30	0.40
e	0.65 BSC		



Suggested Solder Pad Layout
Top View

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.

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