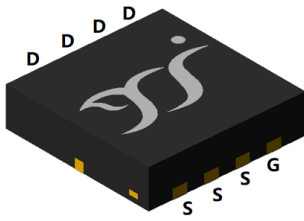
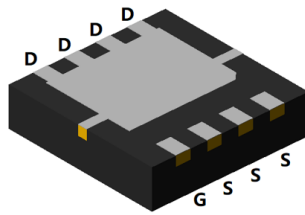


## P-Channel Enhancement Mode Field Effect Transistor

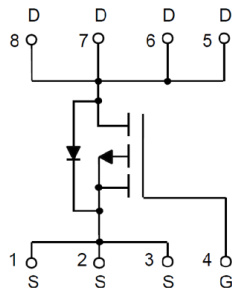


Top View



Bottom View

**DFN3333-8L**



### Product Summary

- $V_{DS}$  -100V
- $I_D$  -15A
- $R_{DS(ON)}$  (at  $V_{GS}=-10V$ ) <110 mohm
- $R_{DS(ON)}$  (at  $V_{GS}=-4.5V$ ) <120 mohm
- 100% EAS Tested

### General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$
- Moisture Sensitivity Level 3
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

### Applications

- DC-DC Converters
- Power management functions

### ■ Absolute Maximum Ratings ( $T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	-100	V
Gate-source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current	$T_A=25^\circ C$	$I_D$	-4.5	A
	$T_A=100^\circ C$		-2.8	
	$T_C=25^\circ C$		-15	
	$T_C=100^\circ C$		-9.5	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	-45	A
Avalanche energy <sup>B</sup>		EAS	64	mJ
Total Power Dissipation <sup>C</sup>	$T_A=25^\circ C$	$P_D$	3	W
	$T_A=100^\circ C$		1.2	
	$T_C=25^\circ C$		43	
	$T_C=100^\circ C$		17.2	
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~+150	$^\circ C$

### ■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient <sup>D</sup>	$t \leq 10S$	$R_{\theta JA}$	20	25	$^\circ C/W$
Thermal Resistance Junction-to-Ambient <sup>D</sup>	Steady-State		40	50	
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	2.4	2.9	

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ15GP10A	F1	Q15GP10A	5000	10000	100000	13" reel



# YJQ15GP10A

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =-250μA	-100			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-100V, V <sub>GS</sub> =0V	T <sub>J</sub> =25°C		-1	μA
			T <sub>J</sub> =55°C		-5	
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1.0	-1.8	-2.5	V
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> = -10V, I <sub>D</sub> =-10A		83	110	mΩ
		V <sub>GS</sub> = -4.5V, I <sub>D</sub> =-5A		95	120	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =-15A, V <sub>GS</sub> =0V			-1.3	V
Maximum Body-Diode Continuous Current	I <sub>S</sub>				-15	A
Gate resistance	R <sub>g</sub>	f=1MHz, Open drain		10		Ω
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-50V, V <sub>GS</sub> =0V, f=1MHZ		1051		pF
Output Capacitance	C <sub>oss</sub>			119		
Reverse Transfer Capacitance	C <sub>rss</sub>			25		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g(-10V)</sub>	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-50V, I <sub>D</sub> =-5A		20.1		nC
Total Gate Charge	Q <sub>g(-4.5V)</sub>			9.7		
Gate-Source Charge	Q <sub>gs</sub>			3.98		
Gate-Drain Charge	Q <sub>gd</sub>			4.38		
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =-5A, di/dt=100A/us		140		nC
Reverse Recovery Time	t <sub>rr</sub>			80		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =-10V, V <sub>DD</sub> =-50V, I <sub>DS</sub> =-5A R <sub>GEN</sub> =6Ω		10		ns
Turn-on Rise Time	t <sub>r</sub>			30		
Turn-off Delay Time	t <sub>D(off)</sub>			77		
Turn-off fall Time	t <sub>f</sub>			81		

A. Repetitive rating; pulse width limited by max. junction temperature.

B. T<sub>J</sub>=25°C, V<sub>DD</sub>=-50V, V<sub>G</sub>=-10V, R<sub>G</sub>=25Ω, L=0.5mH, I<sub>AS</sub>=-16A.

C. Pd is based on max. junction temperature, using junction-case thermal resistance.

D. The value of RθJA is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with TA =25° C. The Power dissipation PDSM is based on RθJA ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.



## ■ Typical Performance Characteristics

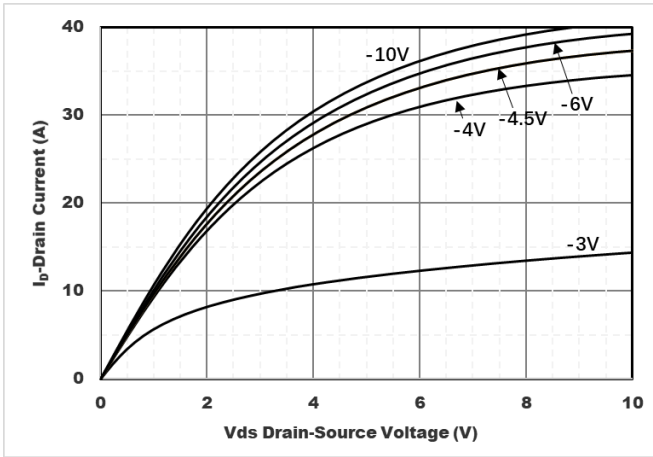


Figure1. Output Characteristics

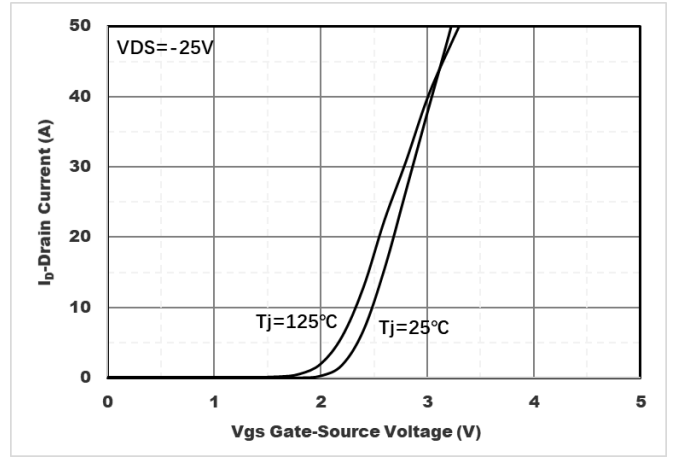


Figure2. Transfer Characteristics

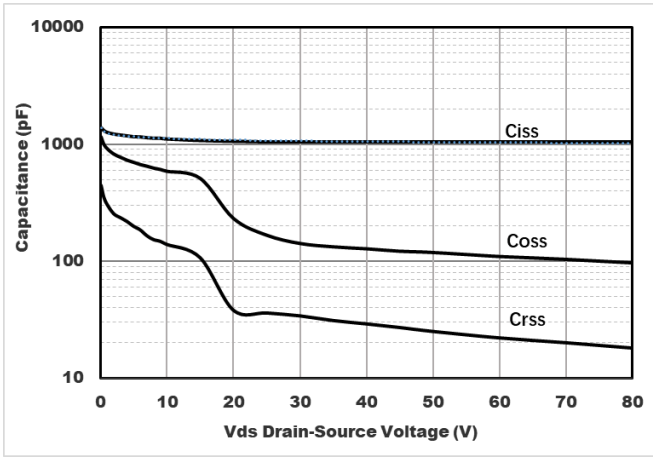


Figure3. Capacitance Characteristics

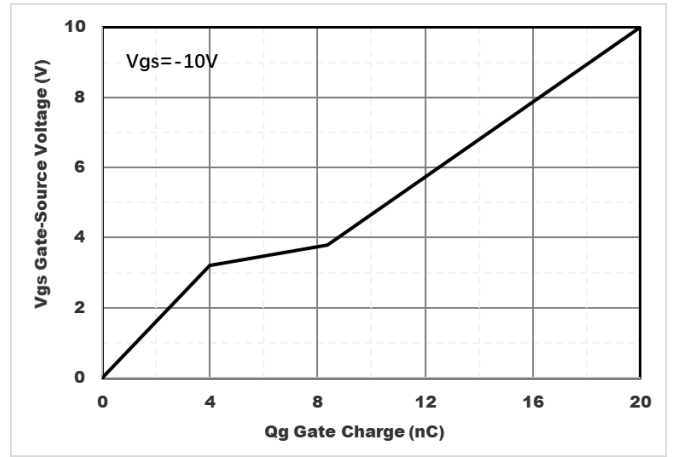


Figure4. Gate Charge

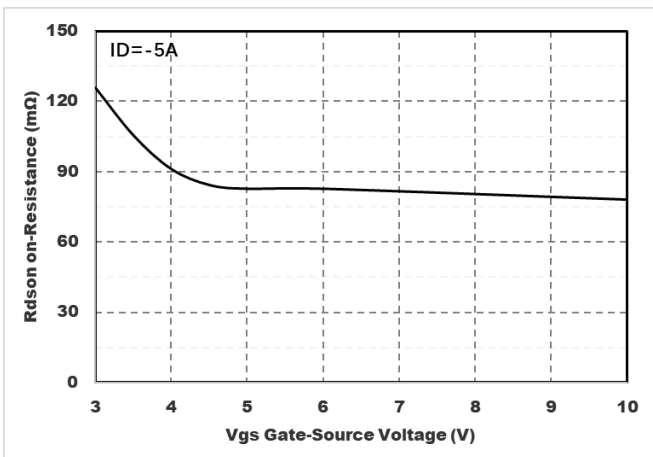


Figure5. : On-Resistance vs. Gate to Source Voltage

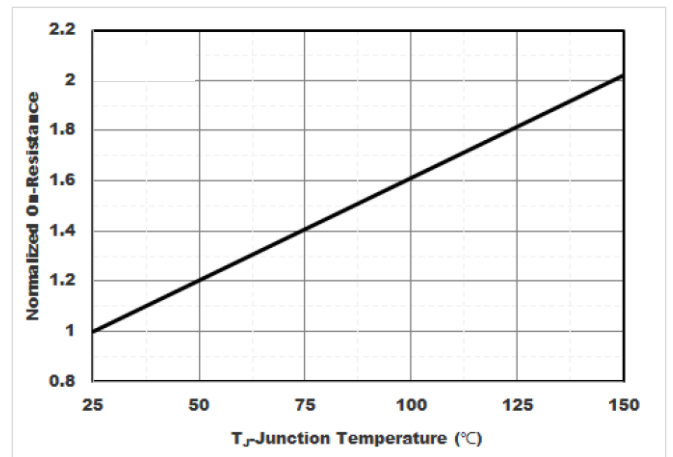


Figure6. Normalized On-Resistance



# YJQ15GP10A

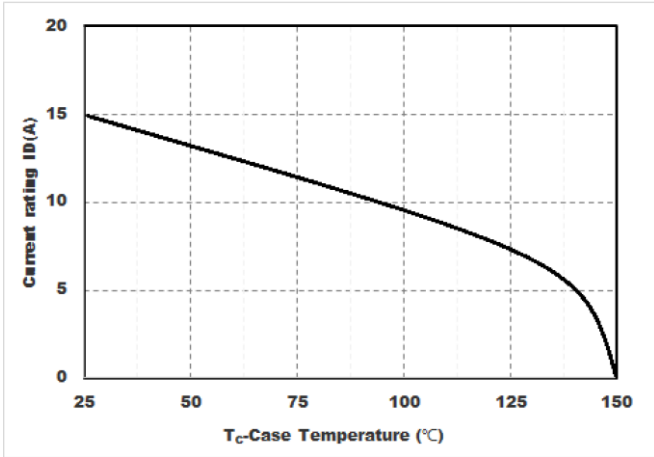


Figure7. Drain current

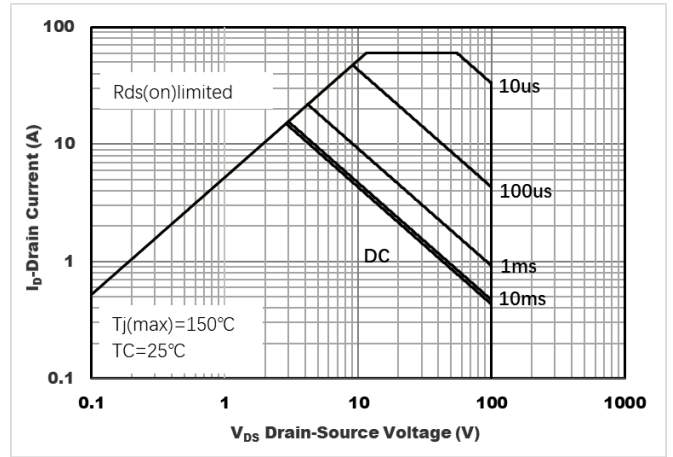


Figure8.Safe Operation Area

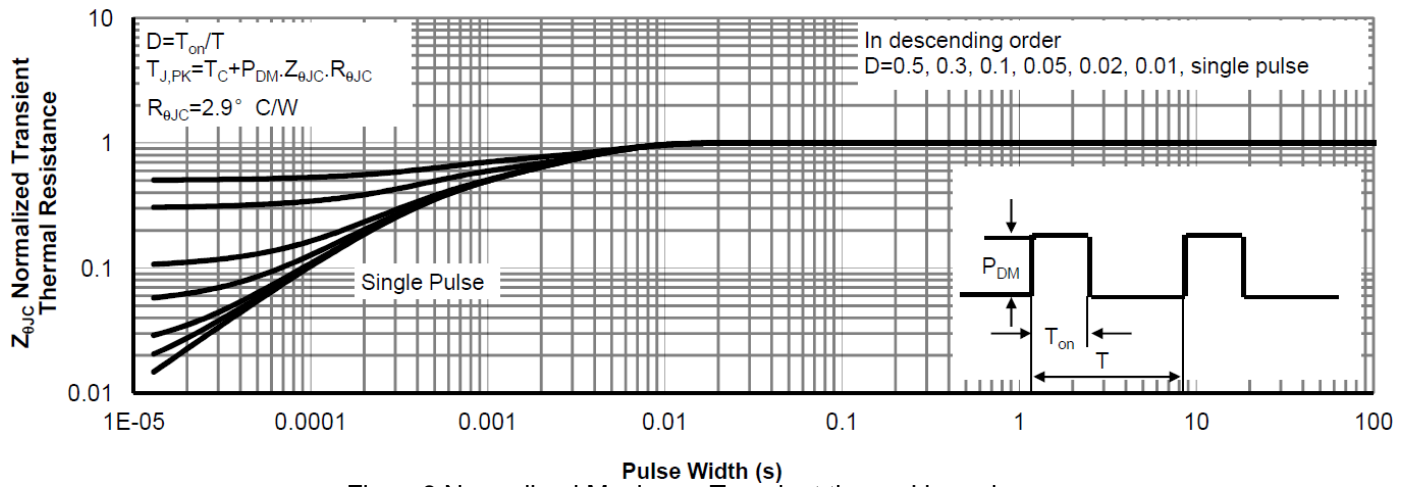
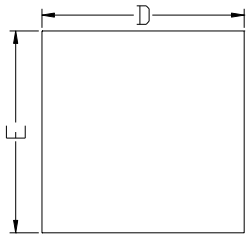


Figure9.Normalized Maximum Transient thermal impedance

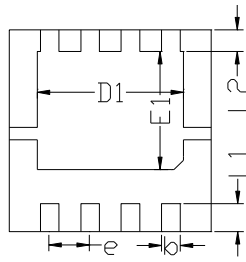


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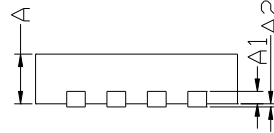
## ■ DFN3333-8L Package Information



Top View  
正面视图

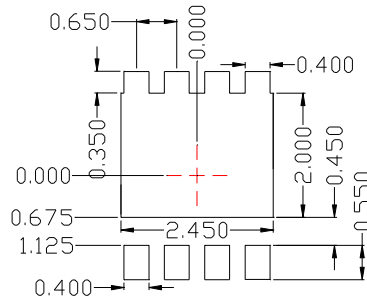


Bottom View  
背面视图



Side View  
侧面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	2.20	2.35	2.50
E1	1.80	1.90	2.00
L1	0.35	0.45	0.55
L2	0.35 BSC		
b	0.20	0.30	0.40
e	0.65 BSC		



Suggested Solder Pad Layout  
Top View

Note:

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.10\text{mm}$ .
3. The pad layout is for reference purposes only.



## YJQ15GP10A

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