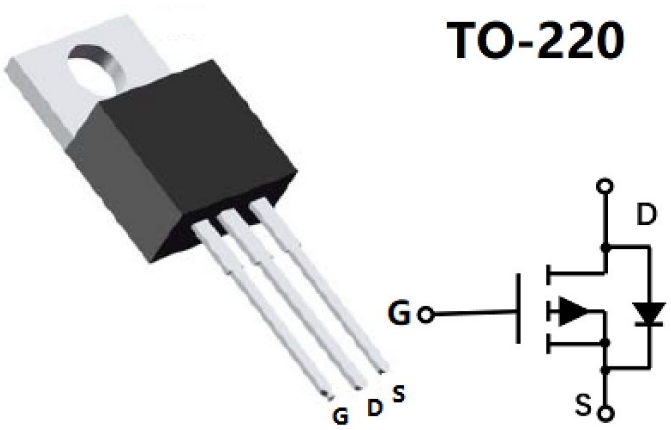
P-Channel Enhancement Mode Field Effect Transistor



Product Summary

- V_{DS} -100V
- I_D -30A
- $R_{DS(ON)}$(at V_{GS}=-10V) ＜56 mohm
- $R_{DS(ON)}$(at V_{GS}=-4.5V) ＜62 mohm
- 100% UIS Tested
- 100% ▽V_{DS} Tested

General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

Applications

- DC-DC Converters
- Power management functions

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	-100	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current	Tc=25℃	I_D	-30	A
	Tc=100℃		-19.2	
Pulsed Drain Current [A]		I_{DM}	-120	A
Avalanche energy [B]		E_{AS}	162	mJ
Total Power Dissipation [C]	Tc=25℃	P_D	125	W
	Tc=100℃		50	
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

■Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient [D]	t≤10S	$R_{\theta JA}$	12	15	℃/W
Thermal Resistance Junction-to-Ambient [D]	Steady-State		50	60	
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	0.8	1.0	

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJP30GP10A	B1	YJP30GP10A	50	/	5000	Tube

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Static Parameter							
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=-250μA		-100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-100V,V_{GS}=0V	T_J=25℃			-1	μA
			T_J=55℃			-5	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V				±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250μA		-1.0	-1.8	-2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= -10V, I_D=-15A			42	56	mΩ
		V_{GS}= -4.5V, I_D=-7A			46	62	
Diode Forward Voltage	V_{SD}	I_S=-15A,V_{GS}=0V				-1.3	V
Maximum Body-Diode Continuous Current	I_S					-30	A
Dynamic Parameters							
Input Capacitance	C_{iss}	V_{DS}=-50V,V_{GS}=0V,f=1MHZ			2100		pF
Output Capacitance	C_{oss}				236		
Reverse Transfer Capacitance	C_{rss}				48		
Switching Parameters							
Total Gate Charge	$Q_{g(-10V)}$	V_{GS}=-10V,V_{DS}=-50V,I_D=-5A			40		nC
Total Gate Charge	$Q_{g(-4.5V)}$				19.4		
Gate-Source Charge	Q_{gs}				7.8		
Gate-Drain Charge	Q_{gd}				8.6		
Reverse Recovery Chrage	Q_{rr}	I_F=-5A, di/dt=100A/us			280		
Reverse Recovery Time	t_{rr}				104		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-10V,V_{DD}=-50V,I_{DS}=-5A R_{GEN}=6Ω			13		
Turn-on Rise Time	t_r				39		
Turn-off Delay Time	$t_{D(off)}$				100.1		
Turn-off fall Time	t_f				105.3		

A. Repetitive rating; pulse width limited by max. junction temperature.
B. V_{DD}=50V, R_G=25Ω, L=0.5mH.
C. Pd is based on max. junction temperature, using junction-case thermal resistance.
D. The value of RθJA is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with TA =25° C. The Power dissipation PDSM is based on RθJA t≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

■ Typical Performance Characteristics

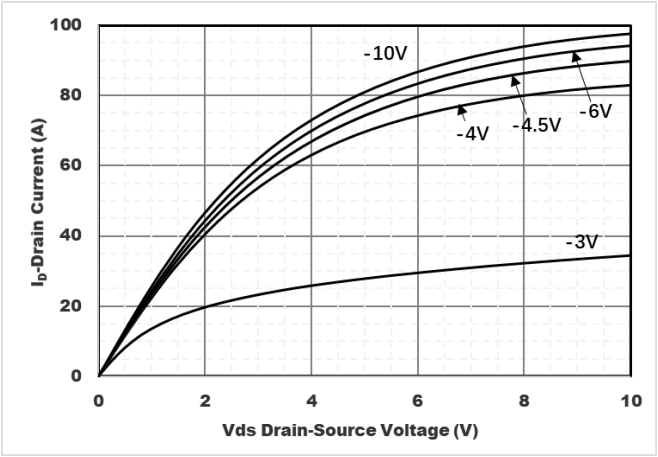


Figure1. Output Characteristics

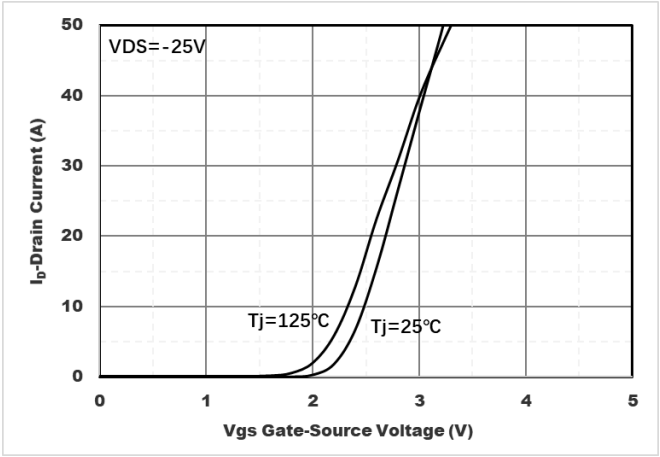


Figure2. Transfer Characteristics

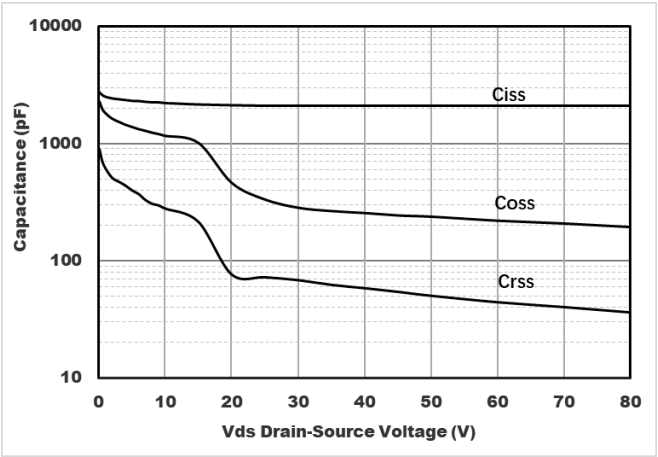


Figure3. Capacitance Characteristics

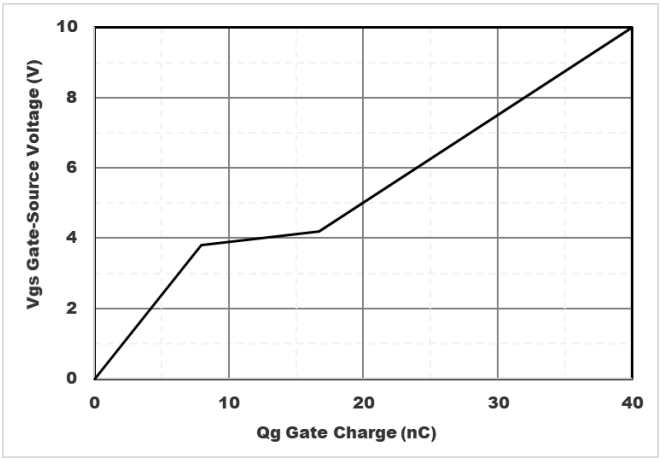


Figure4. Gate Charge

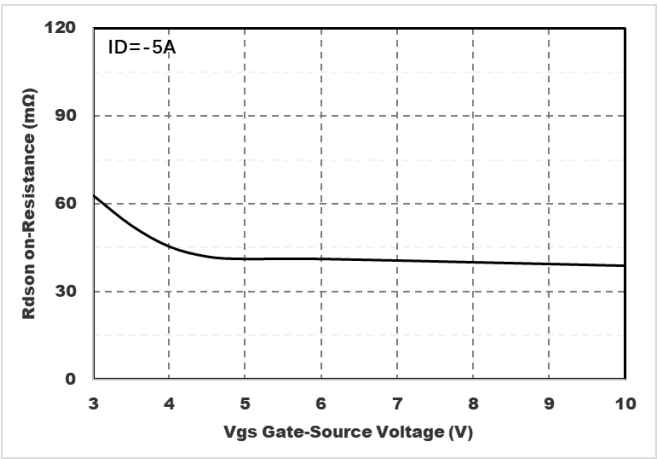


Figure5. : On-Resistance vs. Gate to Source Voltage

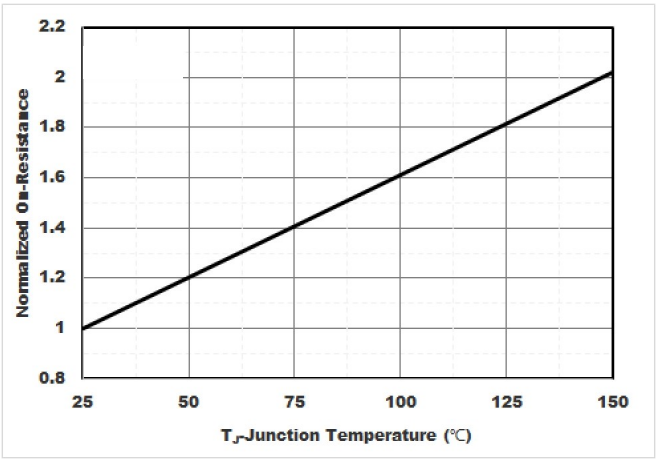


Figure6.Normalized On-Resistance

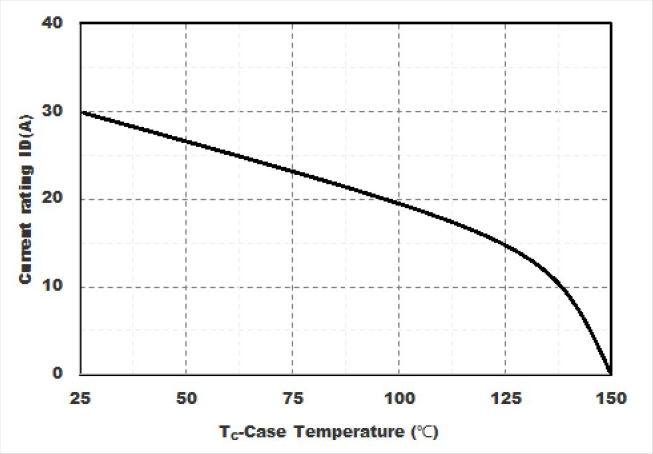


Figure7. Drain current

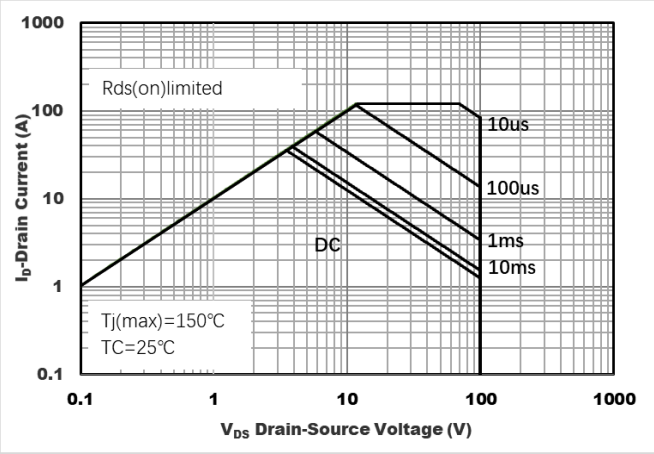


Figure8.Safe Operation Area

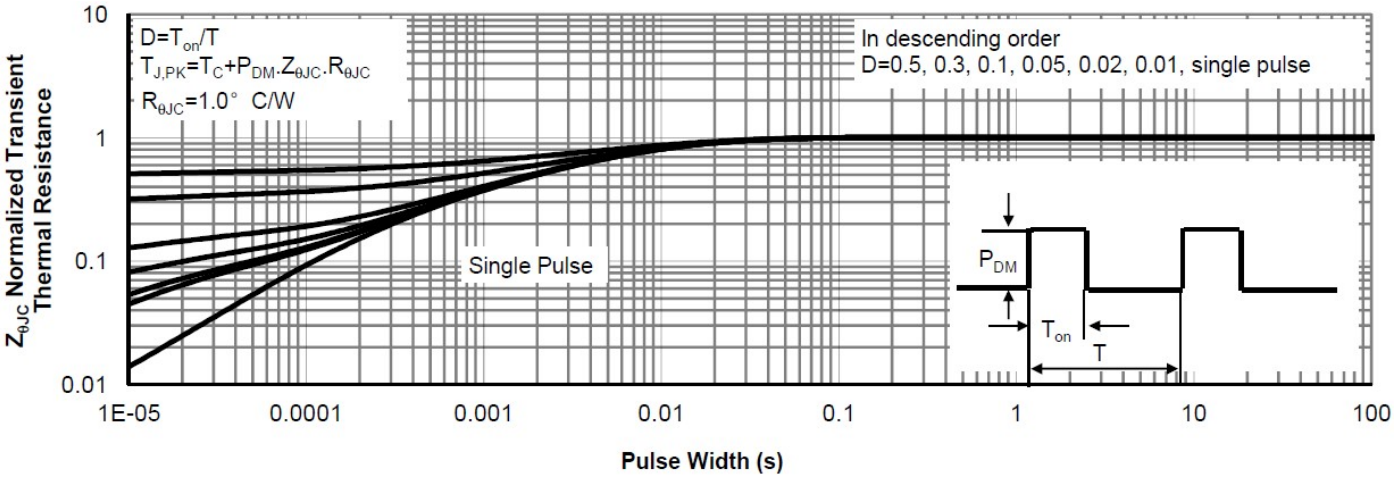
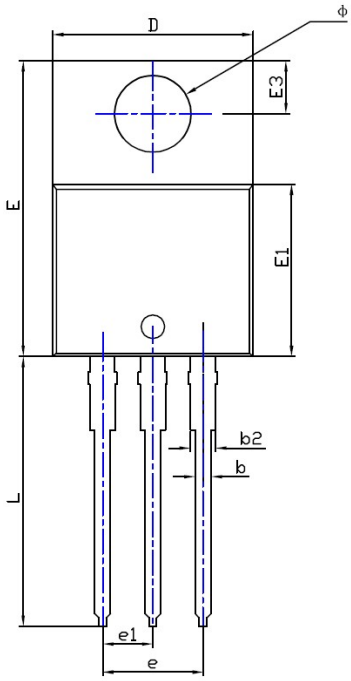
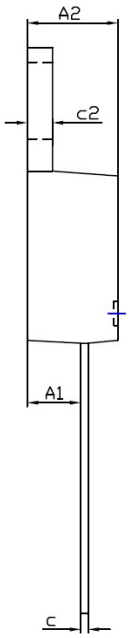


Figure9.Normalized Maximum Transient thermal impedance

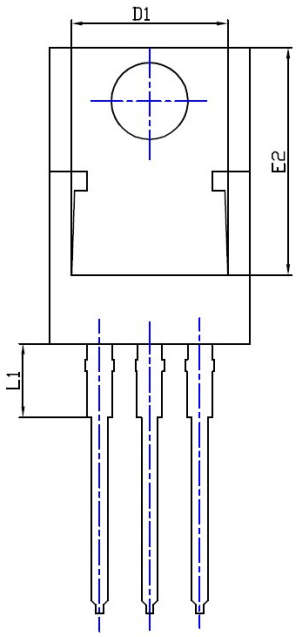
■ TO-220 Package Information



TOP VIEW



SIDE VIEW



BOTTOM VIEW

DIMENSIONS						
SYMBOL	INCHES			Millimeter		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A1	0.098	0.102	0.106	2.480	2.580	2.680
A2	0.174	0.180	0.186	4.430	4.580	4.730
b	0.030	0.032	0.034	0.770	0.820	0.870
b2	0.048	0.050	0.052	1.230	1.280	1.330
c	0.013	0.015	0.018	0.330	0.390	0.450
c2	0.048	0.050	0.053	1.220	1.280	1.340
D	0.394	0.400	0.406	10.000	10.150	10.300
D1	0.299	0.311	0.323	7.600	7.900	8.200
E	0.581	0.587	0.593	14.750	14.900	15.050
E1	0.337	0.341	0.348	8.550	8.700	8.850
E2	0.441	0.453	0.465	11.200	11.500	11.800
E3	0.108BSC			2.750BSC		
e	0.200BSC			5.080BSC		
e1	0.100BSC			2.540BSC		
L	0.531	0.537	0.543	13.500	13.650	13.800
L1	0.152	0.157	0.163	3.850	4.000	4.150
Φ	0.148	0.152	0.156	3.750	3.850	3.950

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

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