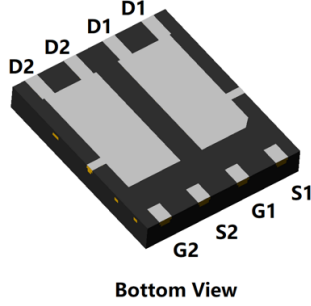
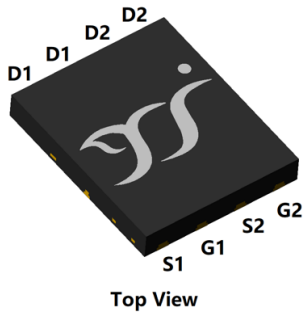
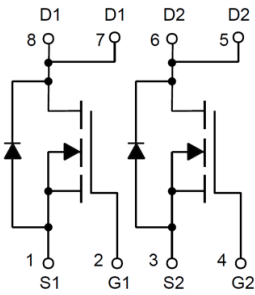


## N-Channel Enhancement Mode Field Effect Transistor



**DFN5060-8L**



### Product Summary

<b>NMOS(Die1)</b>	
• $V_{DS}$	100V
• $I_D$	20A
• $R_{DS(ON)}$ ( at $V_{GS}=10V$ )	<22 mohm
• $R_{DS(ON)}$ ( at $V_{GS}=4.5V$ )	<27 mohm
<b>NMOS(Die2)</b>	
• $V_{DS}$	100V
• $I_D$	20A
• $R_{DS(ON)}$ ( at $V_{GS}=10V$ )	<22 mohm
• $R_{DS(ON)}$ ( at $V_{GS}=4.5V$ )	<27 mohm

### General Description

- Split gate trench MOSFET technology
- High density cell design for low  $R_{DS(ON)}$
- High Speed switching
- Moisture Sensitivity Level 3
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

### Applications

- DC-DC Converters
- Power management functions
- Industrial and Motor Drive application

### ■ Absolute Maximum Ratings ( $T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	N-Die1	N-Die2	Unit
Drain-source Voltage		$V_{DS}$	100	100	V
Gate-source Voltage		$V_{GS}$	$\pm 20$	$\pm 20$	V
Drain Current	$T_C=25^\circ C$	$I_D$	20	20	A
	$T_C=70^\circ C$		12.5	12.5	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	80	80	A
Avalanche energy <sup>B</sup>		$E_{AS}$	64	64	mJ
Total Power Dissipation	$T_C=25^\circ C$	$P_D$	17	17	W
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~+150	-55~+150	$^\circ C$

### ■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient <sup>D</sup>	$t \leq 10S$	$R_{\theta JA}$	30	40	$^\circ C/W$
Thermal Resistance Junction-to-Ambient <sup>D</sup>	Steady-State		60	75	
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	6.2	7.5	

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJGD20G10A	F1	YJGD20G10A	5000	10000	100000	13" reel



# YJGD20G10A

## ■ NMOS(Die1/Die2) Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =250μA	100			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =100V, V <sub>GS</sub> =0V			1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0	1.8	2.5	V
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> =15A		17	22	mΩ
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> =7A		21	27	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =20A, V <sub>GS</sub> =0V		0.96	1.3	V
Maximum Body-Diode Continuous Current	I <sub>S</sub>				20	A
Gate Resistance	R <sub>g</sub>	f=1MHz		1.2		Ω
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =50V, V <sub>GS</sub> =0V, f=1MHZ		1051		pF
Output Capacitance	C <sub>oss</sub>			399		
Reverse Transfer Capacitance	C <sub>rss</sub>			18		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =50V, I <sub>D</sub> =10A		16		nC
Gate-Source Charge	Q <sub>gs</sub>			5.6		
Gate-Drain Charge	Q <sub>gd</sub>			2.4		
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =20A, di/dt=100A/us		42		ns
Reverse Recovery Time	t <sub>rr</sub>			39.8		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =10V, V <sub>DD</sub> =50V, I <sub>D</sub> =4.0A R <sub>GEN</sub> =3.0Ω		39.2		ns
Turn-on Rise Time	t <sub>r</sub>			11		
Turn-off Delay Time	t <sub>D(off)</sub>			53.2		
Turn-off fall Time	t <sub>f</sub>			15.8		
Peak reverse recovery current	I <sub>rm</sub>	I <sub>F</sub> =4A, di/dt=100A/us		3		A

A. Repetitive rating; pulse width limited by max. junction temperature.

B. V<sub>DD</sub>=50V, R<sub>G</sub>=25Ω, L=0.5mH, I<sub>AS</sub>=16A.

C. Pd is based on max. junction temperature, using junction-case thermal resistance.

D. The value of RθJA is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with TA =25° C. The Power dissipation PDSM is based on RθJA ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.



# YJGD20G10A

## ■ NMOS(Die1/Die2) Typical Performance Characteristics

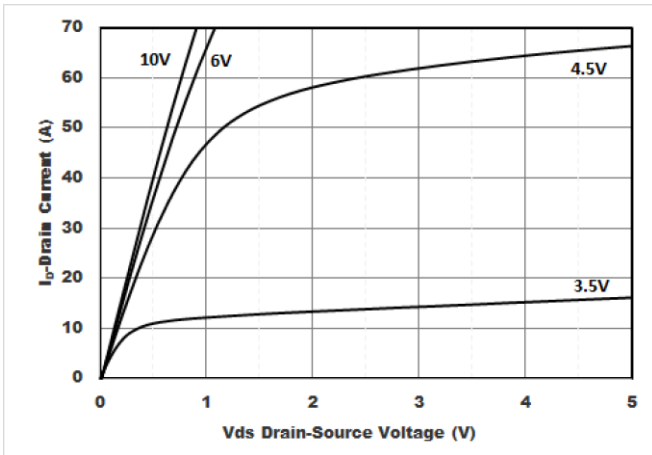


Figure1. Output Characteristics

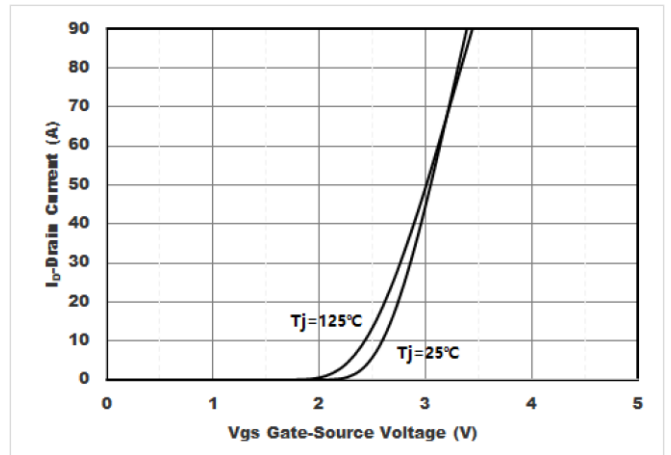


Figure2. Transfer Characteristics

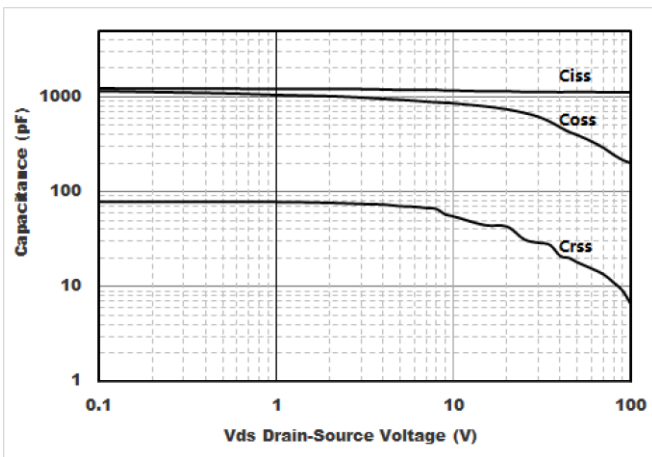


Figure3. Capacitance Characteristics

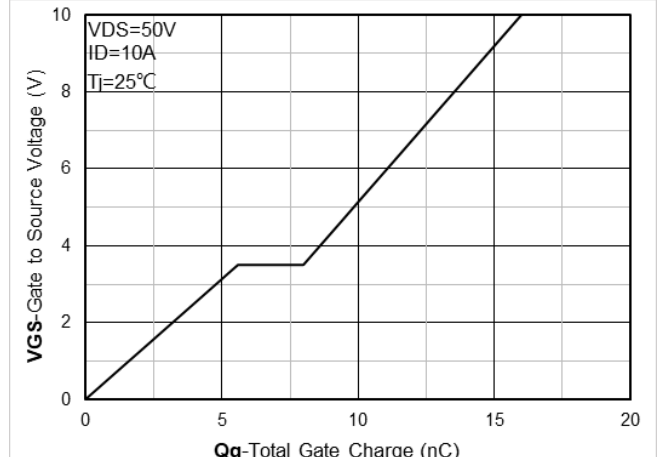


Figure4. Gate Charge

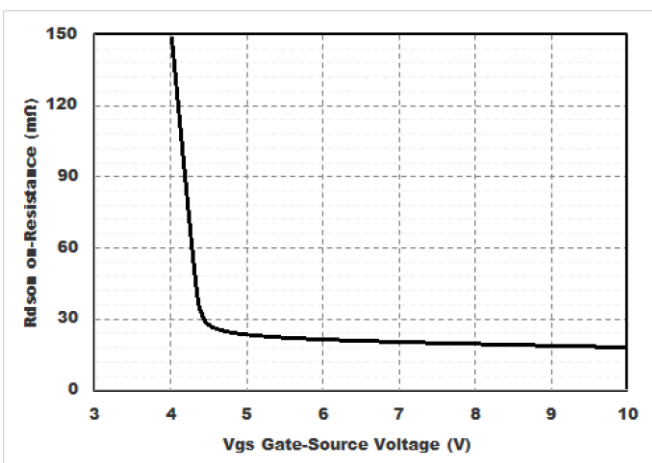


Figure5. : On-Resistance vs. Gate to Source Voltage

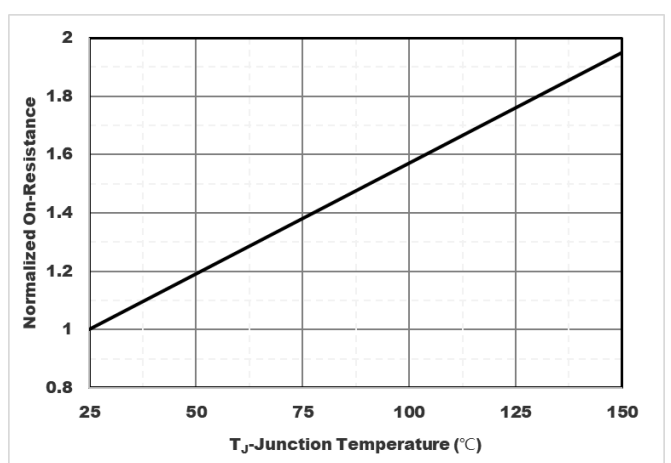


Figure6. Normalized On-Resistance



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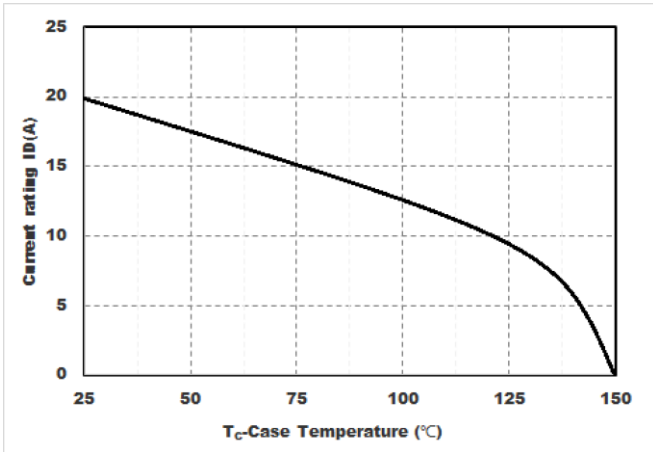


Figure7. Drain current

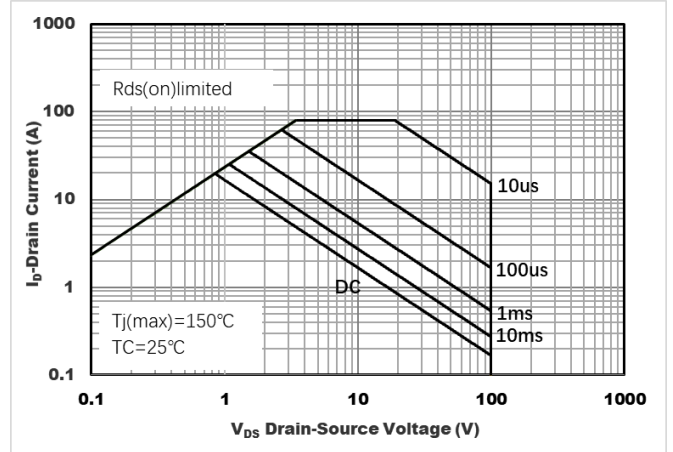


Figure8.Safe Operation Area

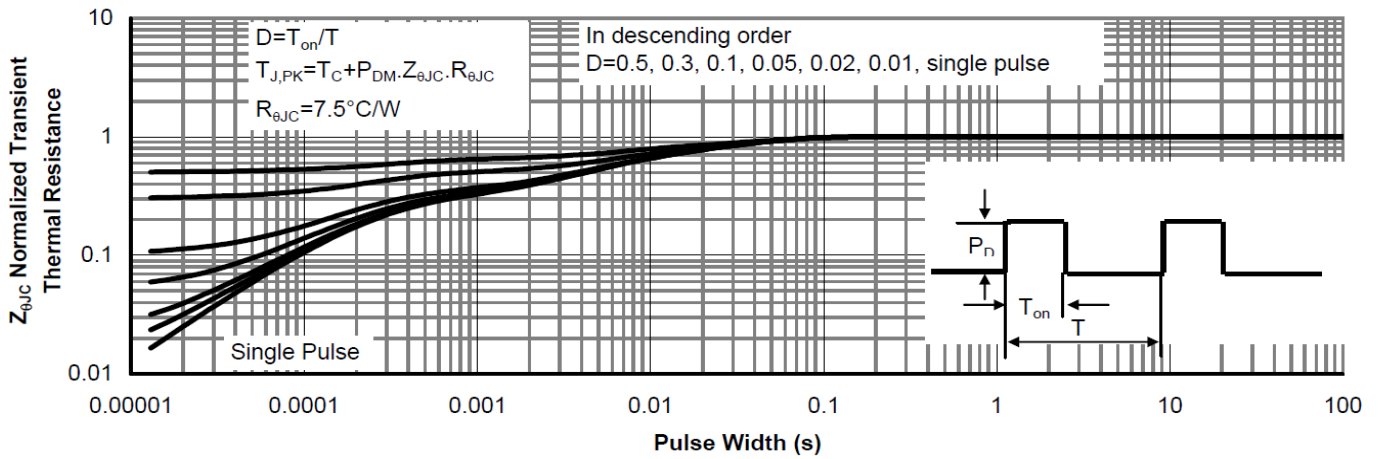
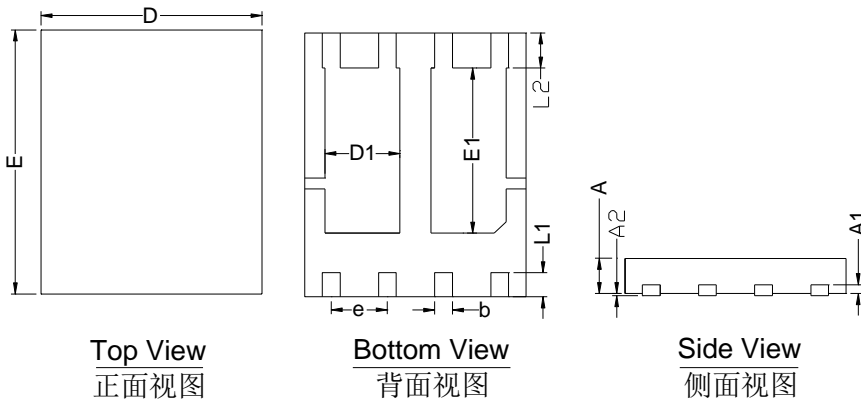


Figure9.Normalized Maximum Transient thermal impedance



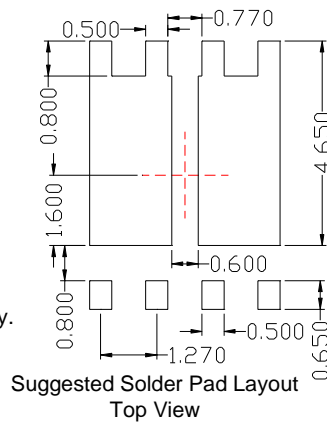
# YJGD20G10A

## ■ DFN5060-8L Package information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	4.90	5.00	5.10
E	5.90	6.00	6.10
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	1.60	1.70	1.80
E1	3.65	3.75	3.85
L1	0.45	0.55	0.65
L2	0.80 BSC		
b	0.30	0.40	0.50
e	1.27 BSC		

- Note:
1. Controlling dimension: in millimeters.
  2. General tolerance:  $\pm 0.10\text{mm}$ .
  3. The pad layout is for reference purposes only.





# YJGD20G10A

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