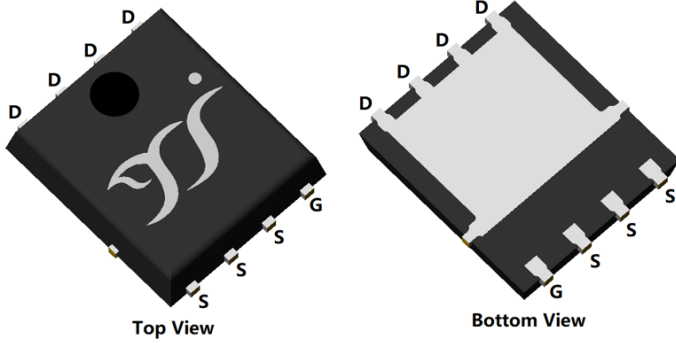
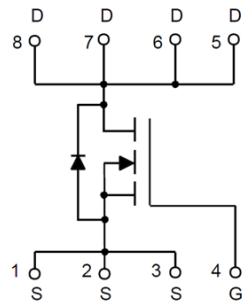


N-Channel Enhancement Mode Field Effect Transistor



Top View

Bottom View



PDFN5060-8L

Product Summary

- V_{DS} 30V
- I_D 40A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) <7.5mohm
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) <11.5mohm
- 100% EAS Tested
- 100% ∇V_{DS} Tested

General Description

- Trench Power LV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 3
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- High current load applications
- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	30	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_C=25^\circ\text{C}$	I_D	40	A
	$T_C=100^\circ\text{C}$		25	
Pulsed Drain Current ^A		I_{DM}	140	A
Total Power Dissipation	$T_C=25^\circ\text{C}$	P_D	21	W
	$T_C=100^\circ\text{C}$		8.4	
Total Power Dissipation	$T_A= -25^\circ\text{C}$	P_D	5	W
Single Pulse Avalanche Energy ^B		E_{AS}	56	mJ
Thermal Resistance Junction-to-Case ^C		$R_{\theta JC}$	6	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction-to-Ambient ^C		$R_{\theta JA}$	25	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ\text{C}$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG40N03A	F1	YJG40N03A	5000	10000	100000	13" reel



YJG40N03A

■ Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	30			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=30V, V_{GS}=0V$			1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$			± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.5	2.5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=15A$		5.5	7.5	m Ω
		$V_{GS}=4.5V, I_D=15A$		9.5	11.5	
Diode Forward Voltage	V_{SD}	$I_S=15A, V_{GS}=0V$		0.85	1.2	V
Gate resistance	R_G	$f=1\text{MHz}$, Open drain	-	1.8	-	Ω
Maximum Body-Diode Continuous Current	I_S				40	A
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$		1015		pF
Output Capacitance	C_{oss}			201		
Reverse Transfer Capacitance	C_{rss}			164		
Gate resistance	R_g	$f=1\text{MHz}$		2.0		Ω
Switching Parameters						
Total Gate Charge	Q_g	$V_{GS}=10V, V_{DS}=15V, I_D=15A$		23.6		nC
Gate-Source Charge	Q_{gs}			3.9		
Gate-Drain Charge	Q_{gd}			7		
Reverse Recovery Charge	Q_{rr}	$I_r=25A, di/dt=100A/us$		0.2		ns
Reverse Recovery Time	t_{rr}			5		
Turn-on Delay Time	$t_{D(on)}$	$V_{GS}=10V, V_{DD}=20V, I_D=2A, R_L=1\Omega$ $R_{GEN}=3\Omega$		7		ns
Turn-on Rise Time	t_r			19		
Turn-off Delay Time	$t_{D(off)}$			24		
Turn-off fall Time	t_f			24		

A. Pulse Test: Pulse Width $\leq 300\mu s$, Duty cycle $\leq 2\%$.

B. $T_J=25^\circ\text{C}$, $V_{DD}=20V$, $V_G=10V$, $L=0.5\text{mH}$, $R_g=25\Omega$, $I_{AS}=15A$

C. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



■ Typical Performance Characteristics

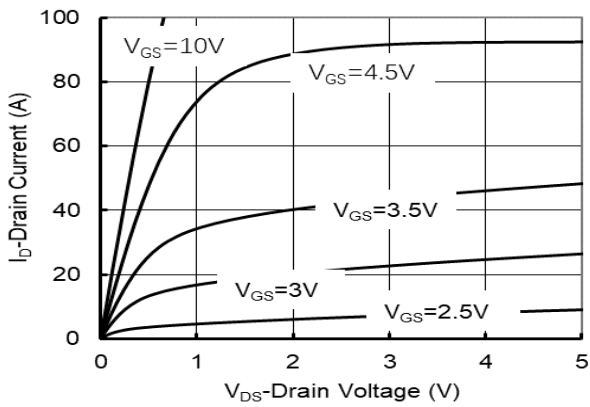


Figure1. Output Characteristics

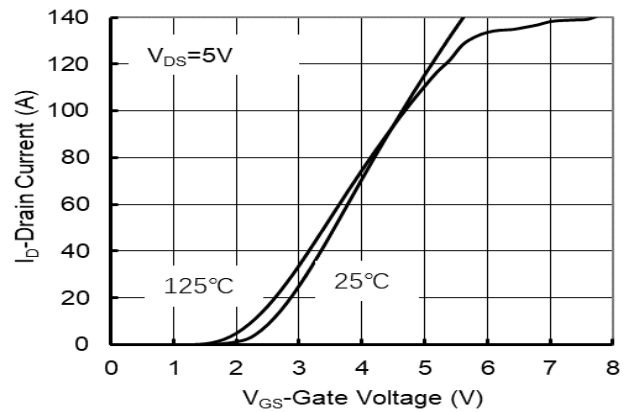


Figure2. Transfer Characteristics

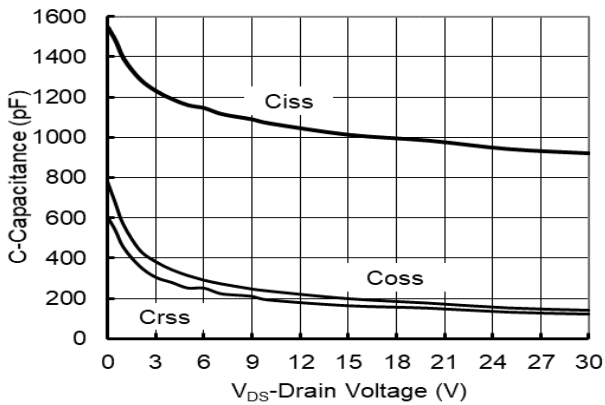


Figure3. Capacitance Characteristics

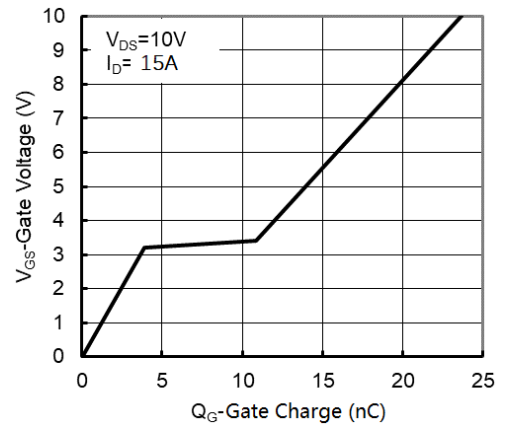


Figure4. Gate Charge

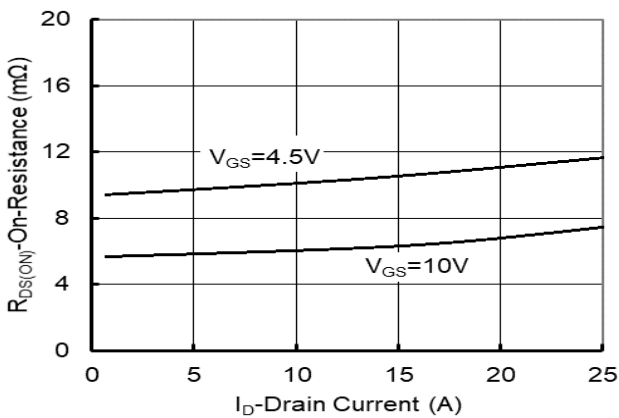


Figure5. Drain-Source on Resistance

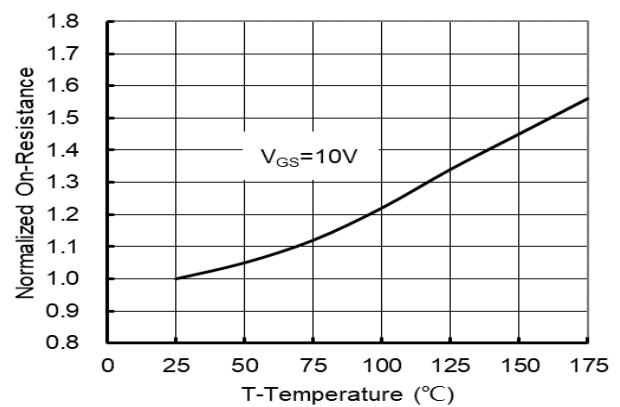


Figure6. Drain-Source on Resistance



YJG40N03A

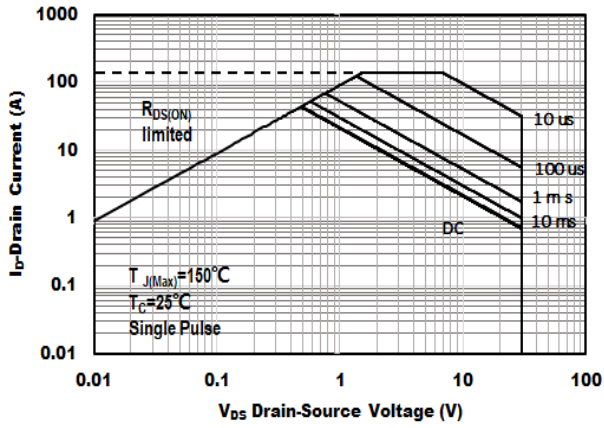


Figure7. Safe Operation Area

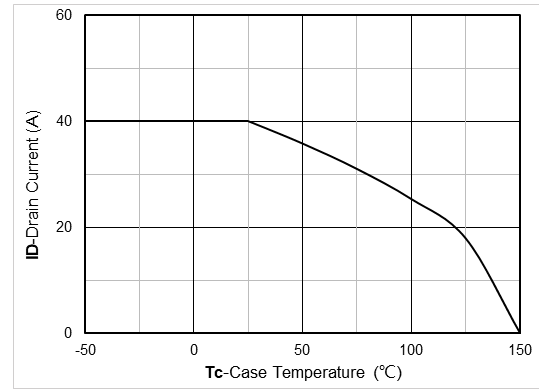


Figure8. Drain current vs. Case Temperature

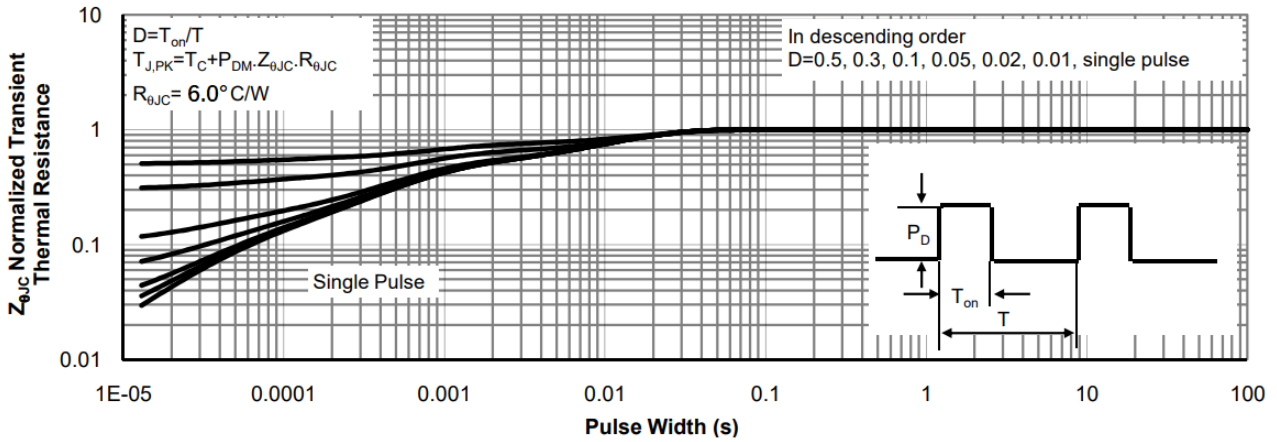
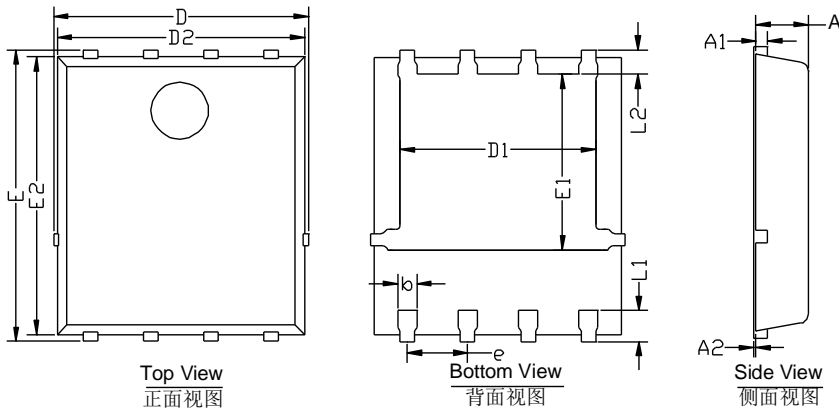


Figure 9. Normalized Maximum Transient Thermal Impedance

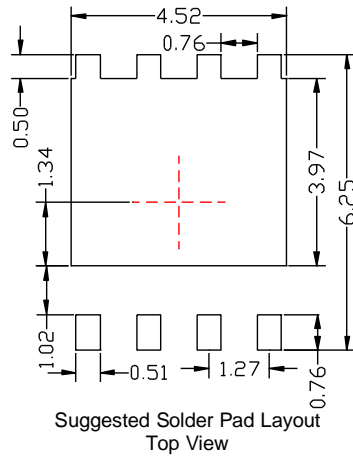


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■ PDFN5060-8L Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		



- Note:
1. Controlling dimension: in millimeters.
 2. General tolerance: $\pm 0.10\text{mm}$.
 3. The pad layout is for reference purposes only.



YJG40N03A

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