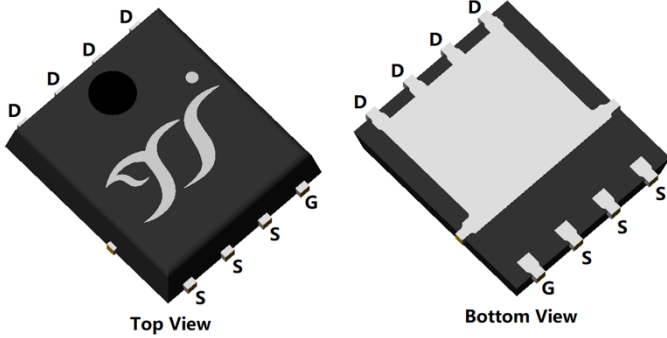
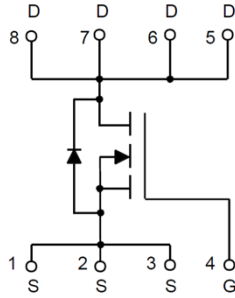


N-Channel Enhancement Mode Field Effect Transistor



Top View

Bottom View



PDFN5060-8L

Product Summary

- V_{DS} 100V
- I_D 18A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) <60mohm
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) <70mohm
- 100% EAS Tested
- 100% ∇V_{DS} Tested

General Description

- Trench Power MV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 3
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- DC-DC Converters
- Power management functions
- Backlighting

■ Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source Voltage	V_{DS}	100	V
Gate-source Voltage	V_{GS}	± 20	V
Drain Current	I_D	$T_A=25^\circ C$	3.5
		$T_A=100^\circ C$	2
		$T_C=25^\circ C$	18
		$T_C=100^\circ C$	11.4
Pulsed Drain Current ^A	I_{DM}	75	A
Total Power Dissipation ^B	P_D	$T_A=25^\circ C$	2
		$T_A=100^\circ C$	0.8
		$T_C=25^\circ C$	45
		$T_C=100^\circ C$	18
Single Pulse Avalanche Energy ^C	E_{AS}	12.5	mJ
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	2.8	$^\circ C/W$
Thermal Resistance Junction-to-Ambient ^D	$R_{\theta JA}$	60	$^\circ C/W$
Junction and Storage Temperature Range	T_J, T_{STG}	-55~+150	$^\circ C$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG18N10A	F1	YJG18N10A	5000	10000	100000	13" reel



YJG18N10A

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	100			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1.1	1.8	3.0	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = 10V, I _D =8A		49	60	mΩ
		V _{GS} = 4.5V, I _D =8A		52	70	
Diode Forward Voltage	V _{SD}	I _S =18A, V _{GS} =0V		0.8	1.2	V
Gate resistance	R _G	f=1MHz, Open drain	-	1.2	-	Ω
Maximum Body-Diode Continuous Current	I _S				18	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, f=1MHZ		2071		pF
Output Capacitance	C _{oss}			73		
Reverse Transfer Capacitance	C _{rss}			54		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =50V, I _D =10A		51.4		nC
Gate-Source Charge	Q _{gs}			9.1		
Gate-Drain Charge	Q _{gd}			11.5		
Reverse Recovery Chrage	Q _{rr}	I _r =10A, di/dt=100A/us		35.3		
Reverse Recovery Time	t _{rr}			38		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =50V, I _D =2A R _{GEN} =3Ω		10		ns
Turn-on Rise Time	t _r			19		
Turn-off Delay Time	t _{D(off)}			42		
Turn-off fall Time	t _f			26		

A. Repetitive rating; pulse width limited by max. junction temperature.

B. P_d is based on max. junction temperature, using junction-case thermal resistance.

C. T_J=25°C, V_{DD}=50V, V_{GS}=10V, L=1mH, I_{AS}=5A.

D. The value of RθJA is measured with the device mounted on 1 in2 FR-4 board with 2oz. Copper, in the still air environment with TA =25°C. The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.



■ Typical Performance Characteristics

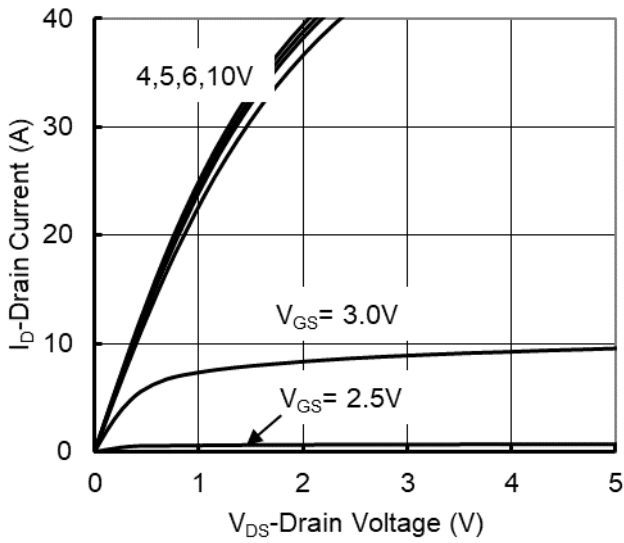


Figure 1. Output Characteristics

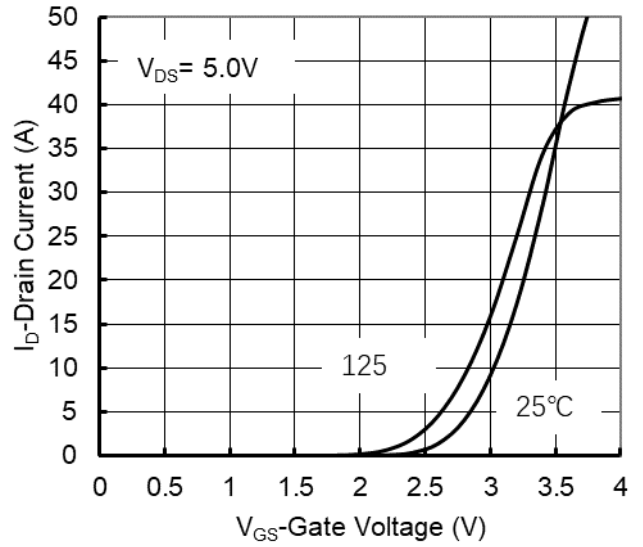


Figure 2. Transfer Characteristics

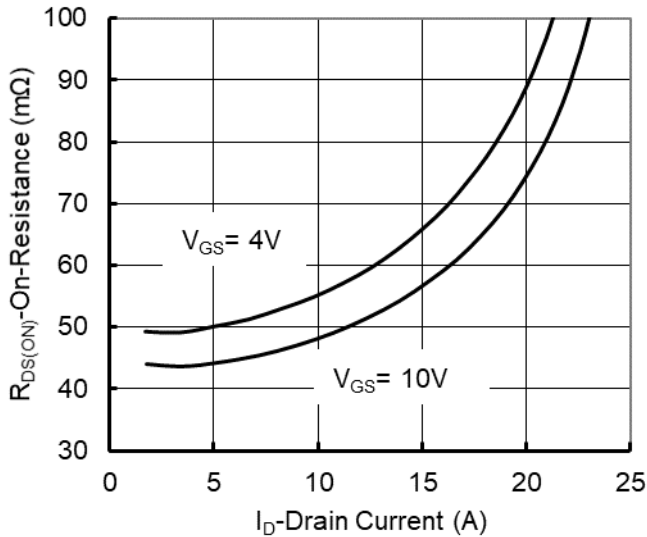


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

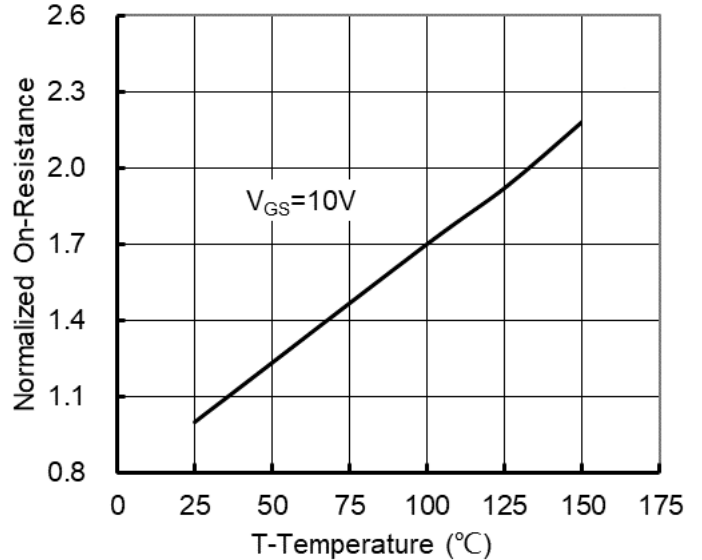


Figure 4. On-Resistance vs. Junction Temperature

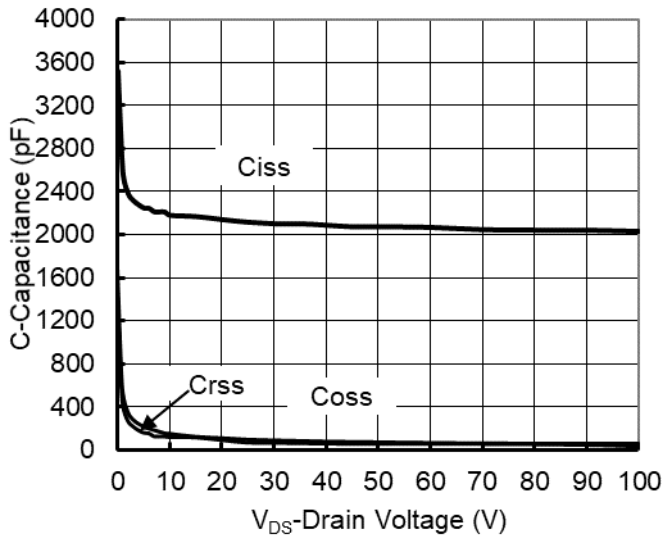


Figure 5. Capacitance Characteristics

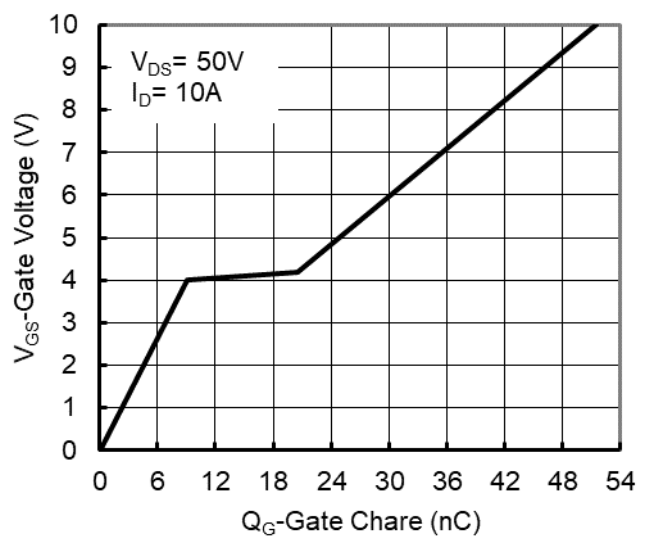


Figure 6. Gate Charge



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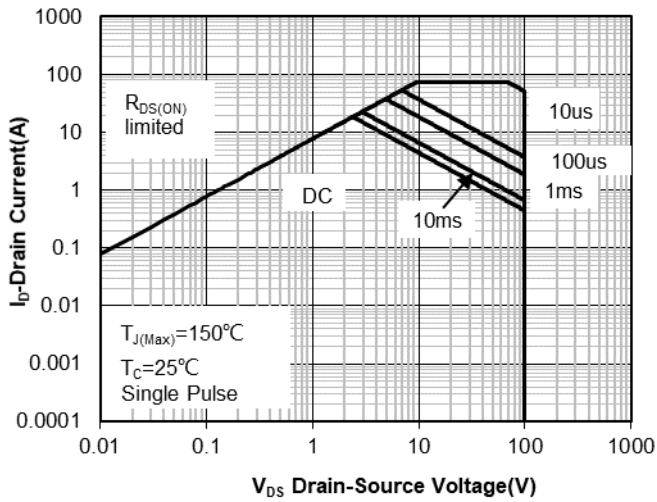


Figure 7. Safe Operation Area

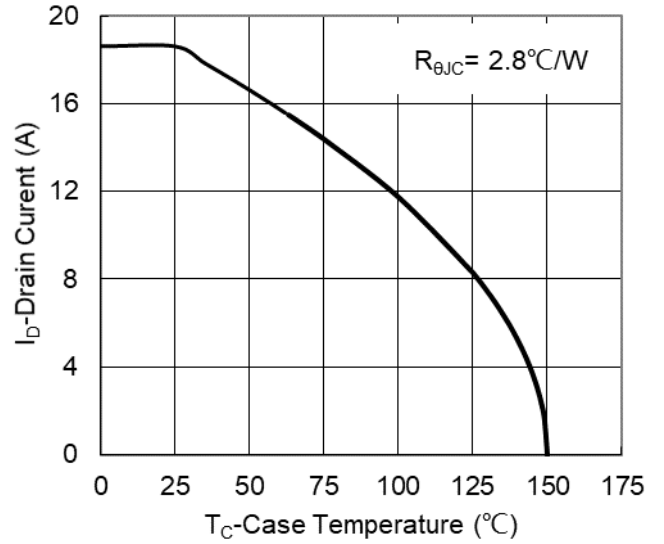


Figure 8. Maximum Continuous Drain Current vs Case Temperature

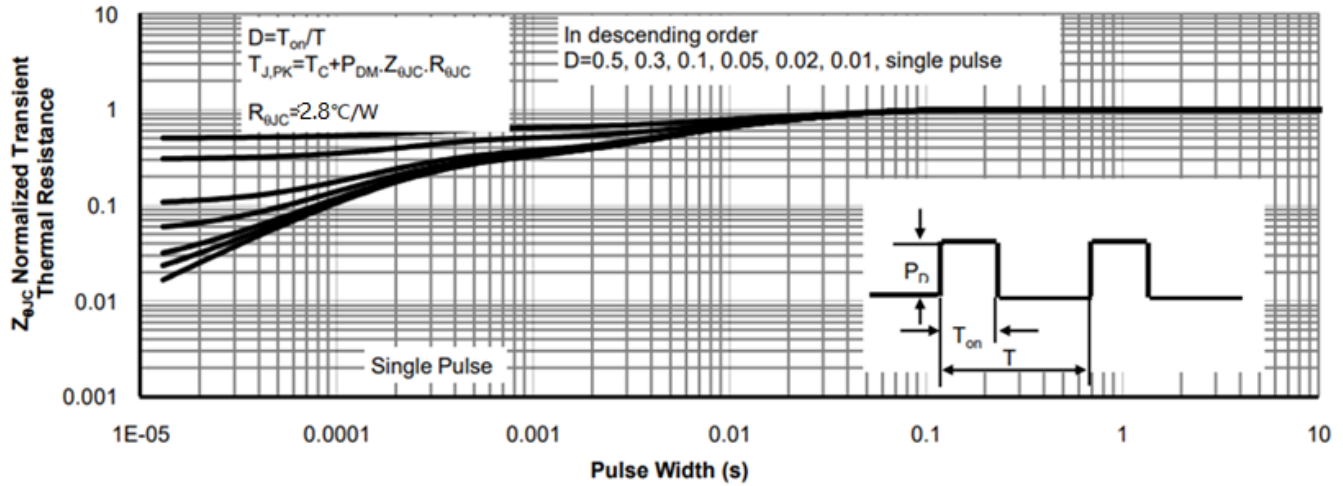
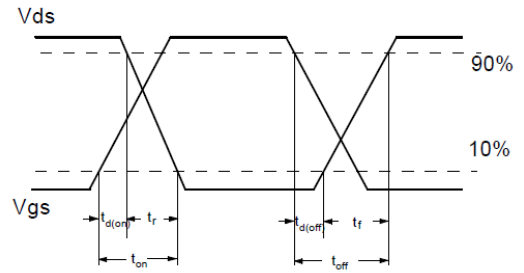
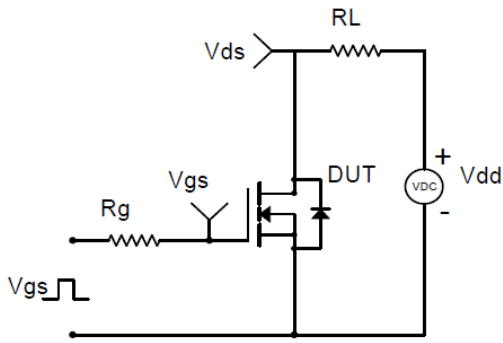
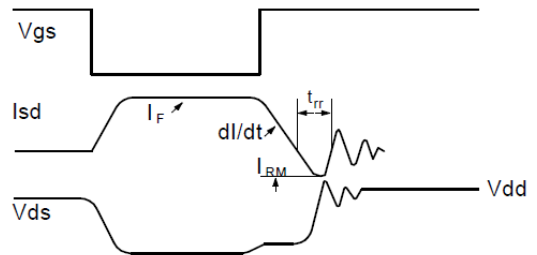
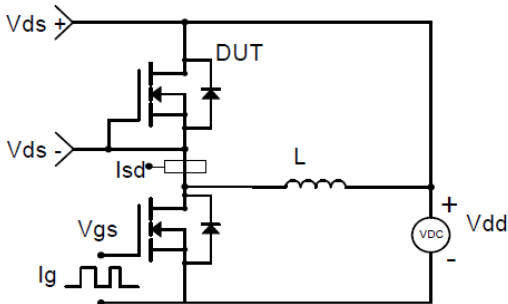


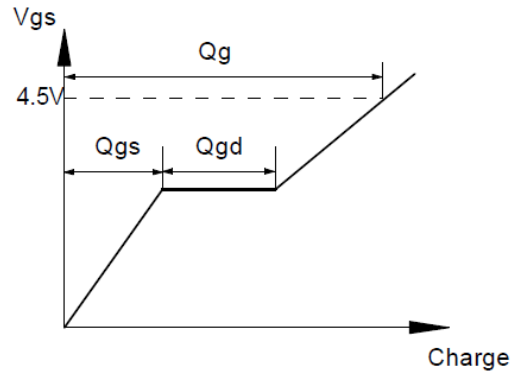
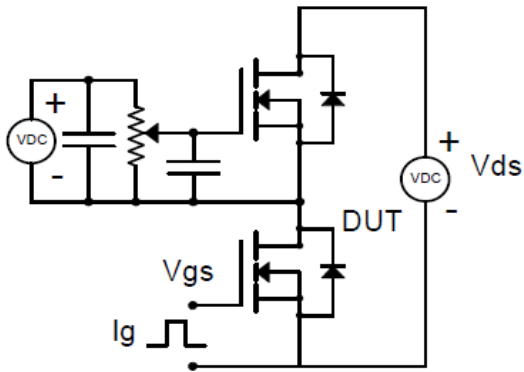
Figure 9. Normalized Maximum Transient Thermal Impedance



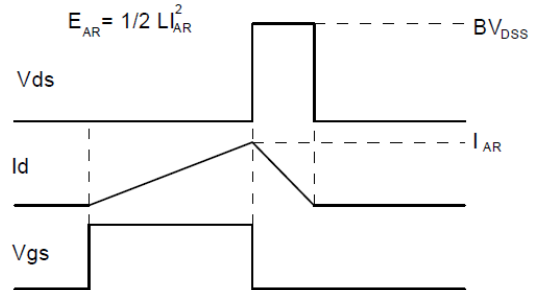
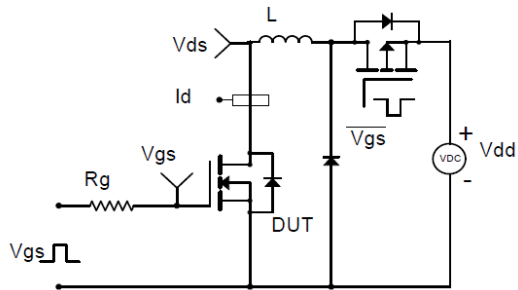
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Gate Charge Test Circuit & Waveform

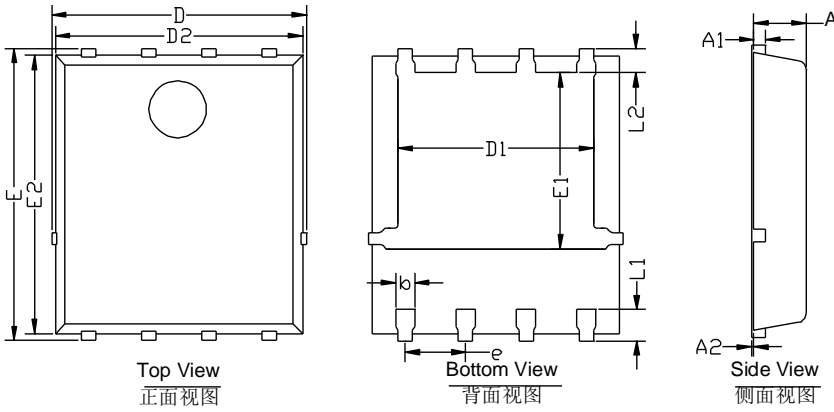


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

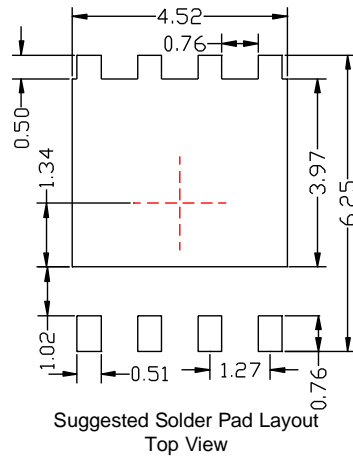


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■ PDFN5060-8L Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		



- Note:
1. Controlling dimension: in millimeters.
 2. General tolerance: ± 0.10 mm.
 3. The pad layout is for reference purposes only.



YJG18N10A

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