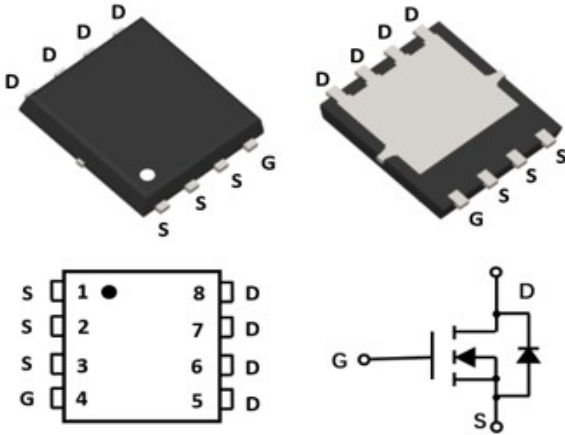


## N-Channel Enhancement Mode Field Effect Transistor

### PDFN 5X6



### Product Summary

- $V_{DS}$  30V
- $I_D$  105A
- $R_{DS(ON)}$  (at  $V_{GS}=10V$ )  $<3.0\text{mohm}$
- $R_{DS(ON)}$  (at  $V_{GS}=4.5V$ )  $<4.0\text{mohm}$
- 100% UIS Tested
- 100%  $\nabla V_{DS}$  Tested

### General Description

- Trench Power MV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$

### Applications

- DC-DC Converters
- Power management functions
- Backlighting

### ■ Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source Voltage	$V_{DS}$	30	V
Gate-source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current	$I_D$	$T_C=25^\circ\text{C}$	105
		$T_C=100^\circ\text{C}$	66
Pulsed Drain Current <sup>A</sup>	$I_{DM}$	415	A
Total Power Dissipation @ $T_C=25^\circ\text{C}$	$P_D$	70	W
Single Pulse Avalanche Energy <sup>B</sup>	$E_{AS}$	507	mJ
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	1.8	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55~+150	$^\circ\text{C}$

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG105N03A	F1	YJG105N03A	5000	10000	100000	13" reel



# YJG105N03A

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =250μA	30			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V			1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0	1.5	2.5	V
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> =20A		2.45	3.0	mΩ
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> =15A		2.9	4.0	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =20A, V <sub>GS</sub> =0V		0.85	1.2	V
Maximum Body-Diode Continuous Current	I <sub>S</sub>				105	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1MHZ		4401		pF
Output Capacitance	C <sub>oss</sub>			581		
Reverse Transfer Capacitance	C <sub>rss</sub>			439		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =20V, I <sub>D</sub> =20A		49.5		nC
Gate-Source Charge	Q <sub>gs</sub>			10.4		
Gate-Drain Charge	Q <sub>gd</sub>			8.9		
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =20A, di/dt=500A/us		7.5		
Reverse Recovery Time	t <sub>rr</sub>			23		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =10V, V <sub>DD</sub> =15V, I <sub>D</sub> =2A, R <sub>GEN</sub> =3Ω		13		ns
Turn-on Rise Time	t <sub>r</sub>			22		
Turn-off Delay Time	t <sub>D(off)</sub>			63		
Turn-off fall Time	t <sub>f</sub>			33		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design, while R<sub>θJA</sub> is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



■ Typical Performance Characteristics

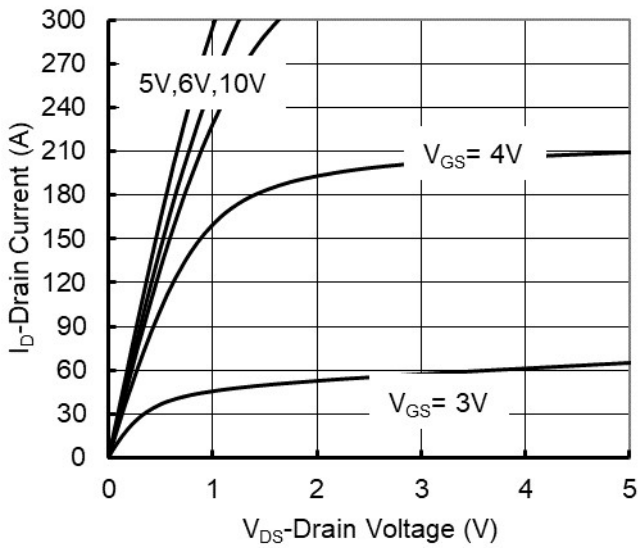


Figure 1. Output Characteristics

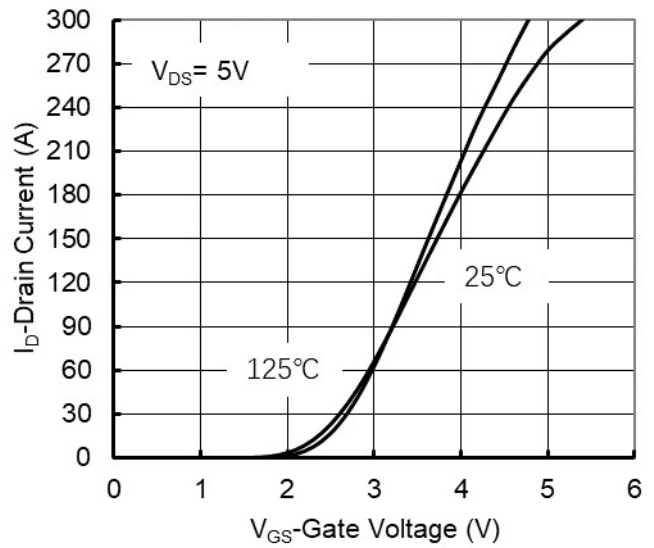


Figure 2. Transfer Characteristics

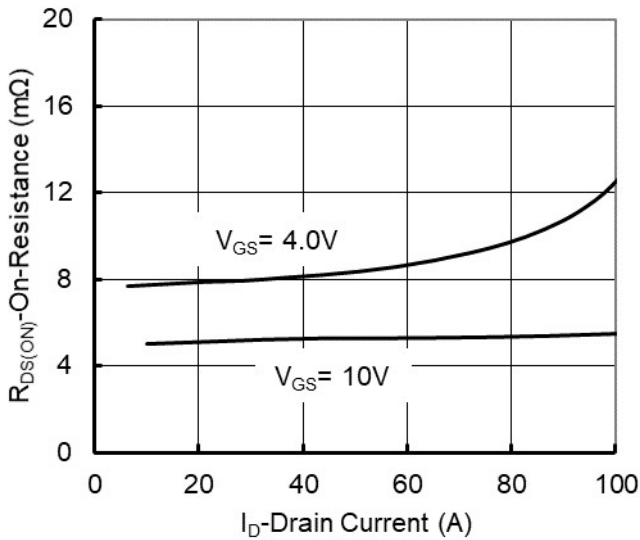


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

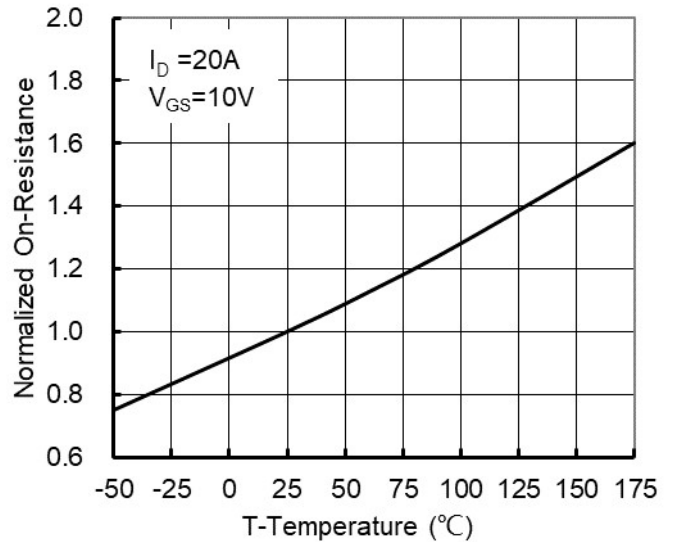


Figure 4. On-Resistance vs. Junction Temperature

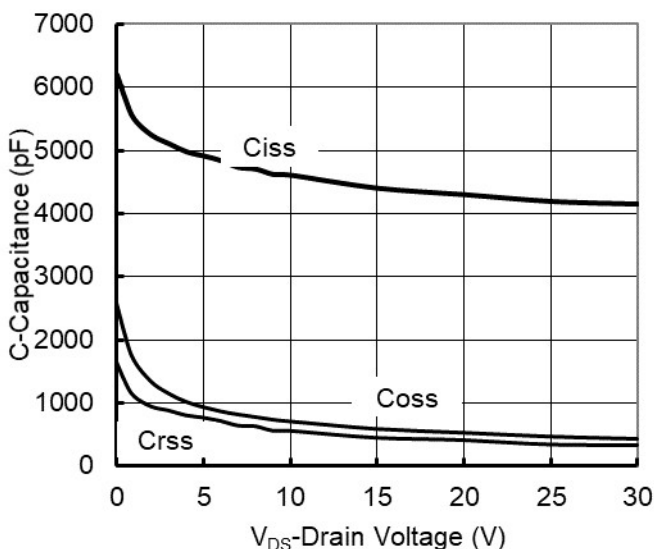


Figure 5. Capacitance Characteristics

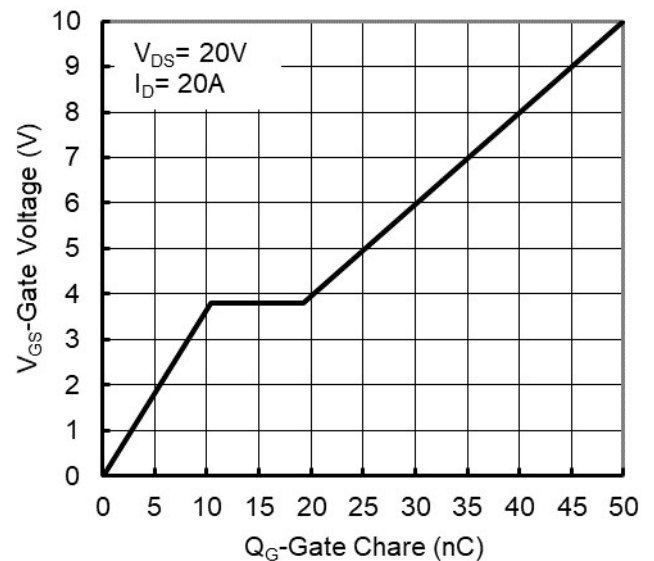


Figure 6. Gate Charge



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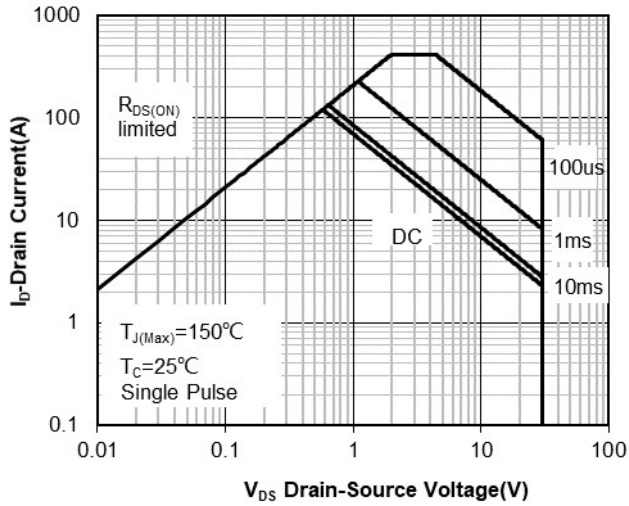


Figure 7. Safe Operation Area

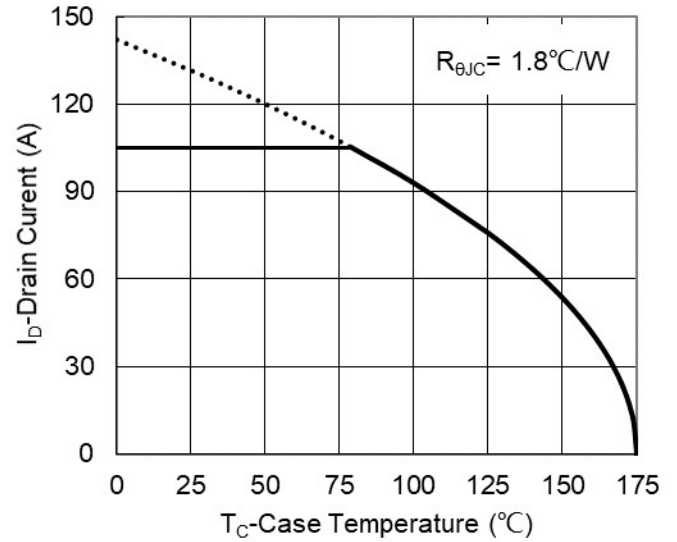


Figure 8. Maximum Continuous Drain Current vs Case Temperature

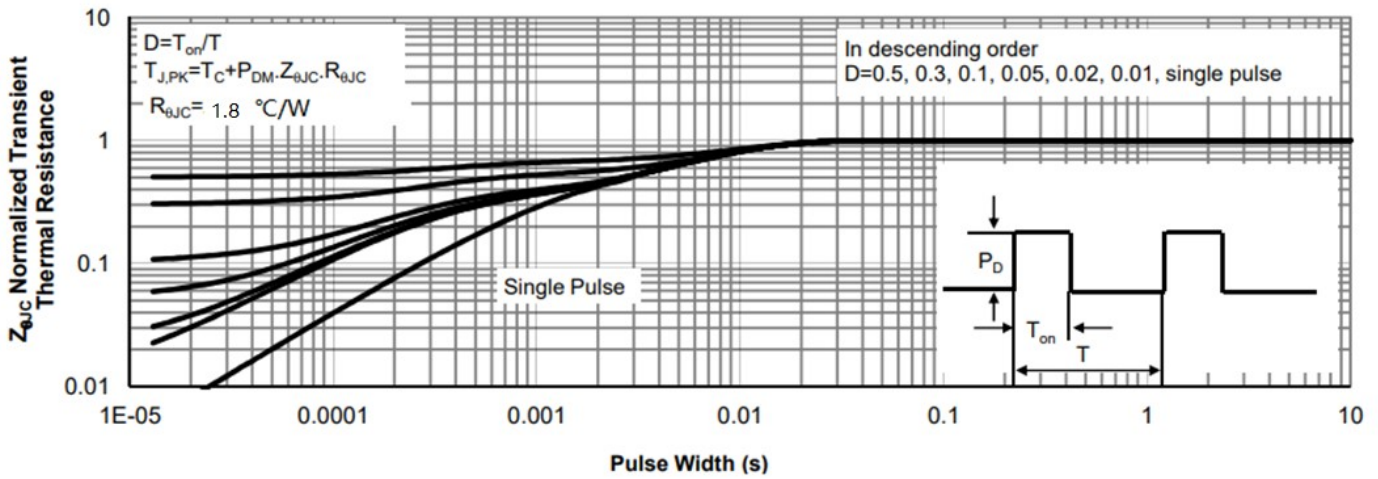
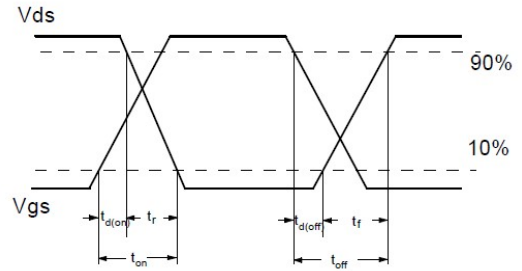
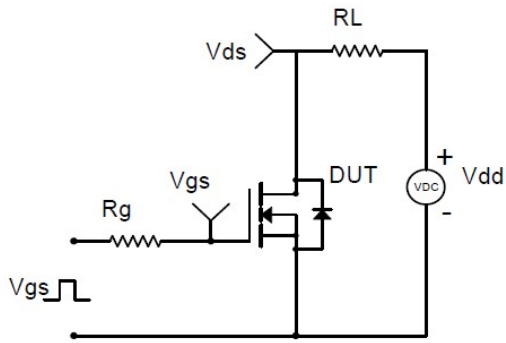
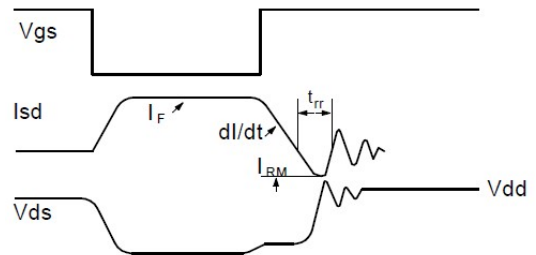
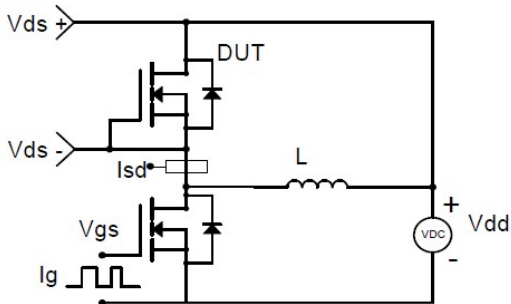


Figure 9. Normalized Maximum Transient Thermal Impedance



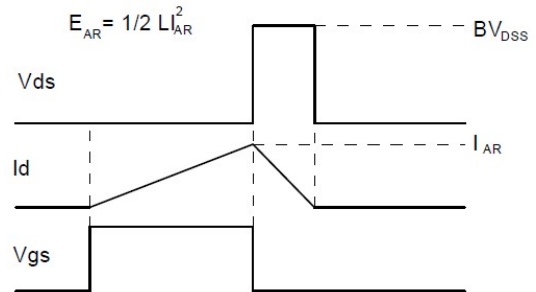
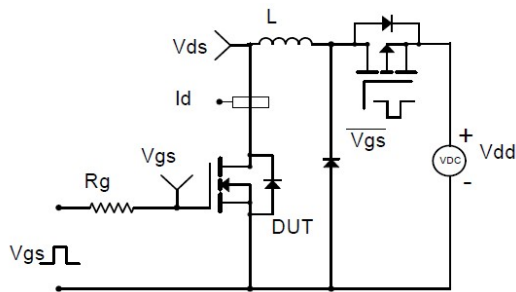
**Resistive Switching Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**



**Gate Charge Test Circuit & Waveform**

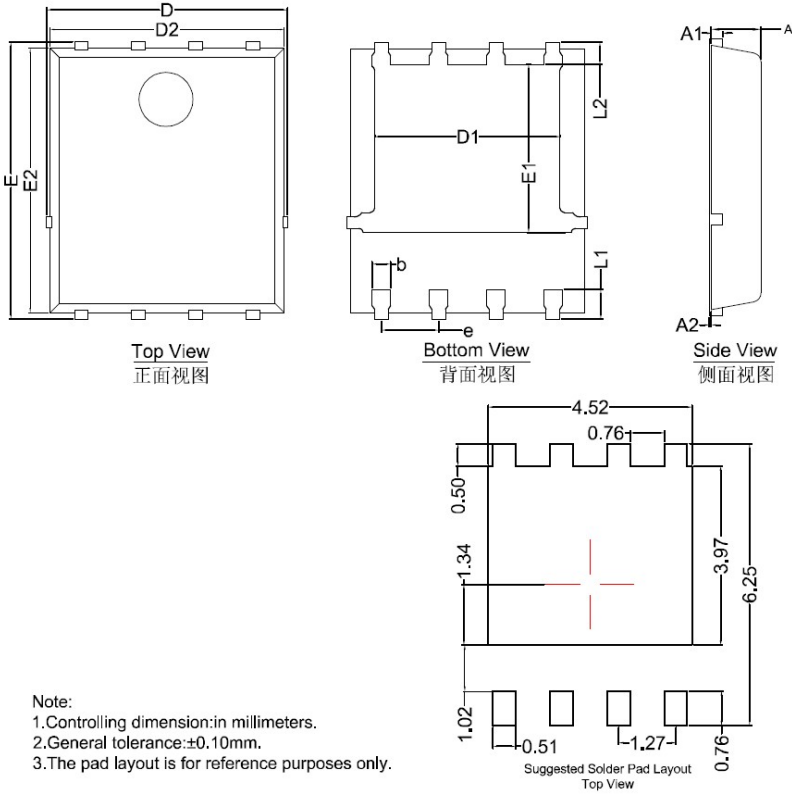


**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**



# YJG105N03A

## ■ PDFN5X6 Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		

Note:  
 1. Controlling dimension: in millimeters.  
 2. General tolerance:  $\pm 0.10$ mm.  
 3. The pad layout is for reference purposes only.



## YJG105N03A

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