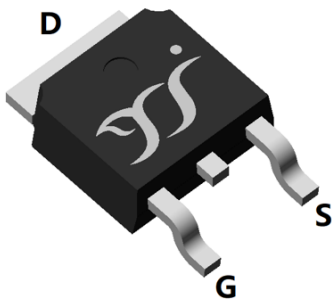
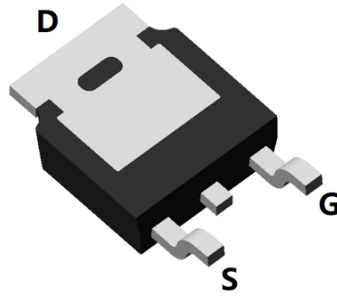


N-Channel Enhancement Mode Field Effect Transistor

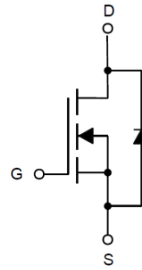


Top View



Bottom View

TO-252



Product Summary

- V_{DS} 30V
- I_D 80A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) < 4.9mohm
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) < 7.0mohm
- 100% EAS Tested
- 100% ∇V_{DS} Tested

General Description

- Trench Power LV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- High current load applications
- Load switch
- Hard switched and high frequency circuits
- Uninterruptible power supply

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source Voltage	V_{DS}	30	V
Gate-source Voltage	V_{GS}	± 20	V
Drain Current	I_D	$T_C=25^\circ\text{C}$	80
		$T_C=100^\circ\text{C}$	50
Pulsed Drain Current ^A	I_{DM}	190	A
Single Pulse Avalanche Energy ^B	E_{AS}	100	mJ
Total Power Dissipation ^C	P_D	$T_C=25^\circ\text{C}$	38
		$T_C=100^\circ\text{C}$	15
Thermal Resistance Junction-to-Ambient ^D	$R_{\theta JA}$	60	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	3.3	
Junction and Storage Temperature Range	T_J, T_{STG}	-55~+150	$^\circ\text{C}$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJD80N03B	F1/F2	YJD80N03B	2500	/	25000	13" reel



YJD80N03B

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1	1.5	2.5	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =20A		3.4	4.9	mΩ
		V _{GS} = 4.5V, I _D =15A		5.4	7.0	
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V		0.85	1.2	V
Gate resistance	R _G	f=1MHz, Open drain	-	2.7	-	Ω
Maximum Body-Diode Continuous Current	I _S				80	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V, f=1MHZ		2191		pF
Output Capacitance	C _{oss}			300		
Reverse Transfer Capacitance	C _{rss}			247		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =15V, I _D =20A		46.3		nC
Gate-Source Charge	Q _{gs}			8.8		
Gate-Drain Charge	Q _{gd}			9.2		
Reverse Recovery Chrage	Q _{rr}	I _r =20A, di/dt=100A/us		1.6		
Reverse Recovery Time	t _{rr}			11		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =15V, R _L =0.75Ω R _{GEN} =3Ω		11		ns
Turn-on Rise Time	t _r			80		
Turn-off Delay Time	t _{D(off)}			39		
Turn-off fall Time	t _f			92		

A. Repetitive rating; pulse width limited by max. junction temperature.

B. T_J=25°C, V_{DD}=50V, V_G=10V, R_G=25Ω, L=0.5mH, I_{AS}=20A.

C. P_d is based on max. junction temperature, using junction-case thermal resistance.

D. The value of R_{θJA} is measured with the device mounted on the minimum recommend pad size, in the still air environment with T_A =25°C. The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.



■ Typical Performance Characteristics

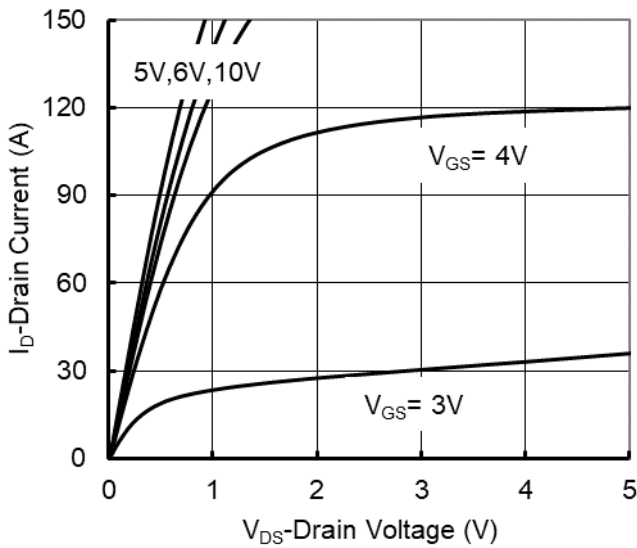


Figure 1. Output Characteristics

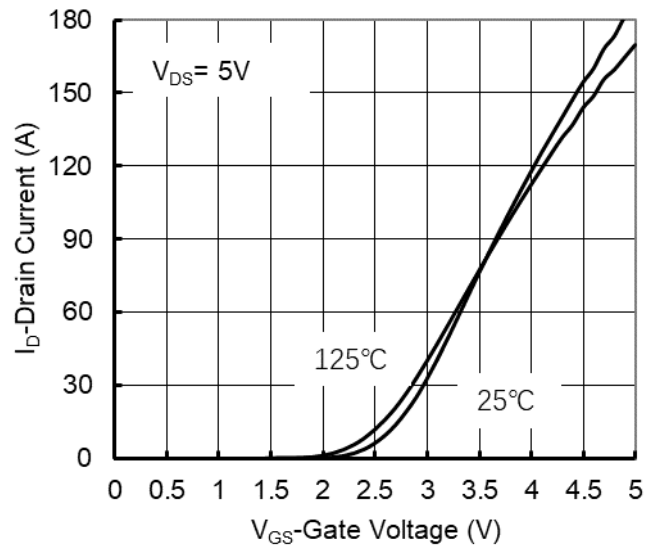


Figure 2. Transfer Characteristics

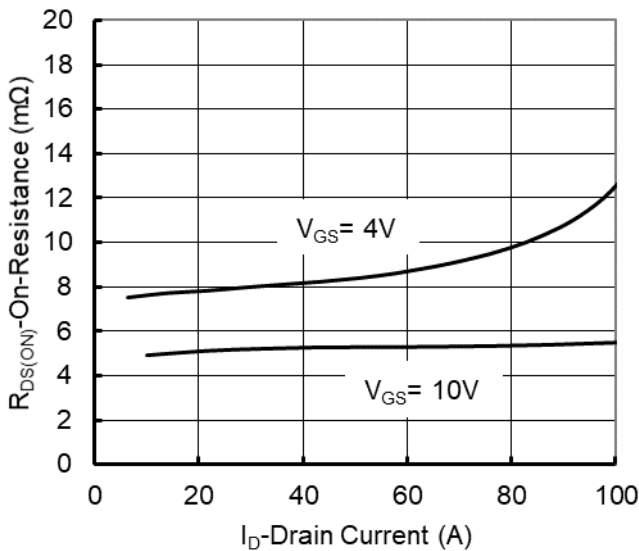


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

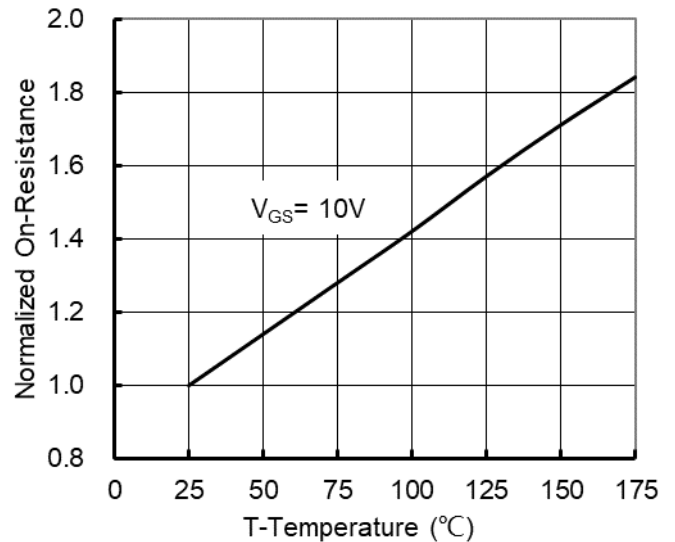


Figure 4. On-Resistance vs. Junction Temperature

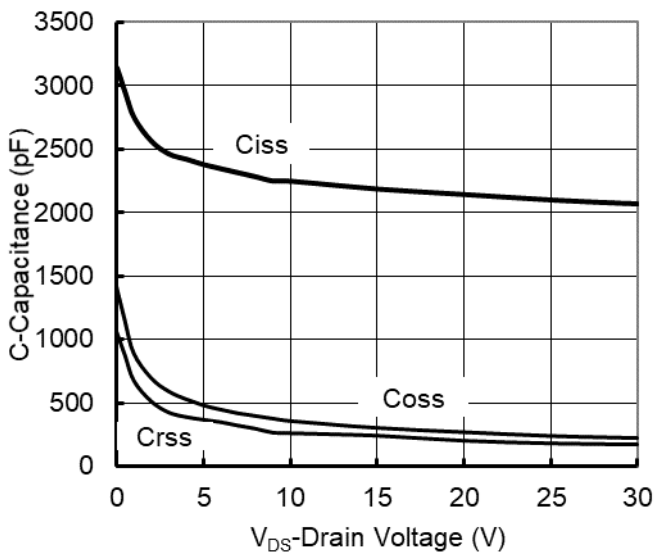


Figure 5. Capacitance Characteristics

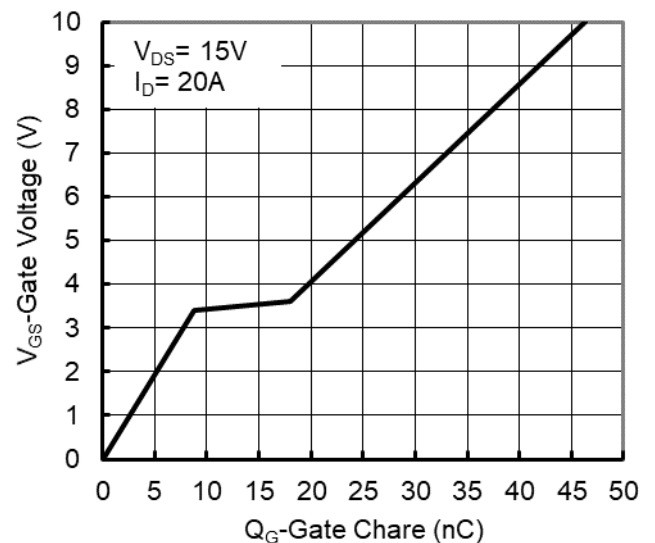


Figure 6. Gate Charge

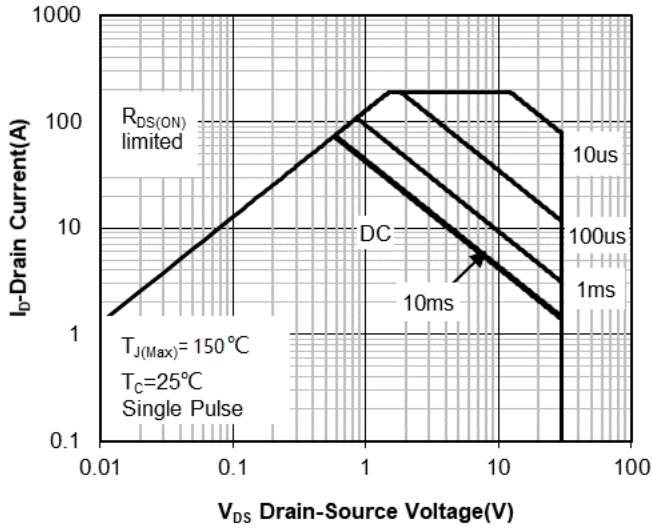


Figure 7. Safe Operation Area

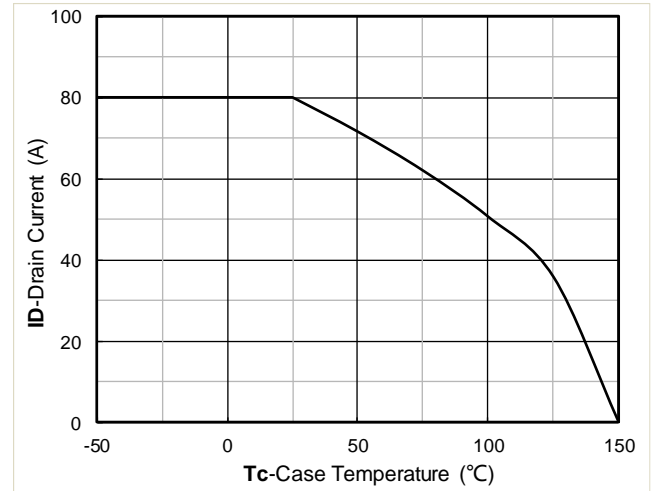


Figure 8. Maximum Continuous Drain Current vs Case Temperature

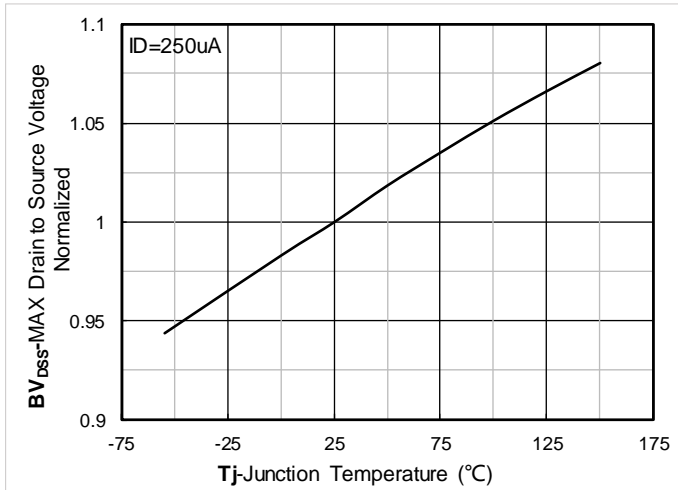


Figure 9. Normalized breakdown voltage

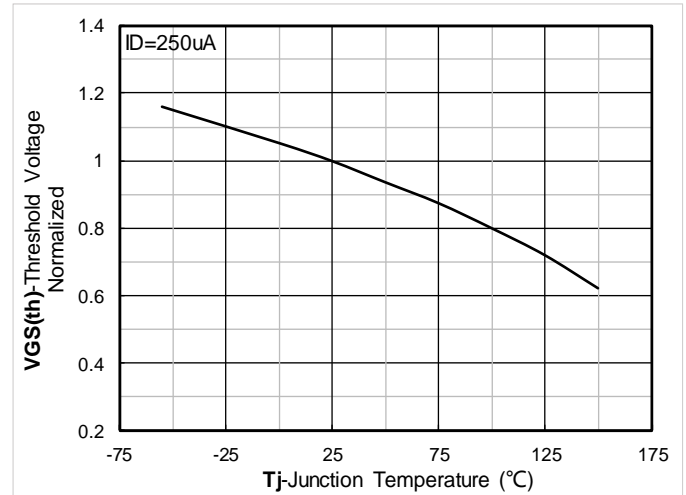


Figure 10. Normalized Threshold voltage

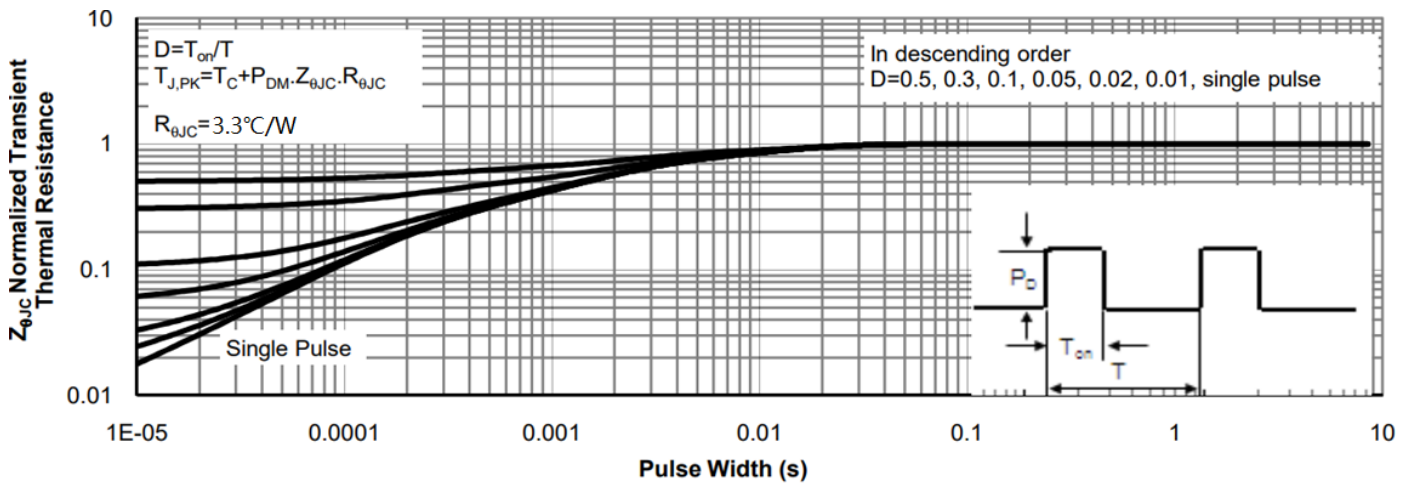
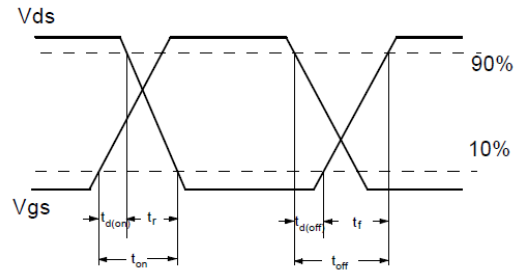
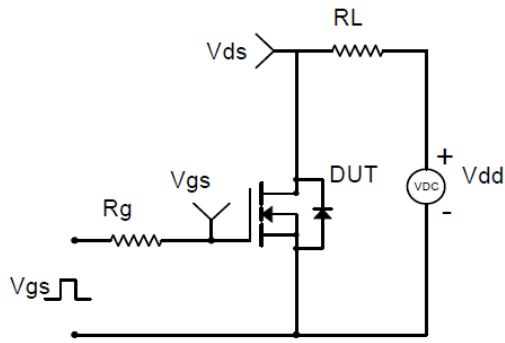
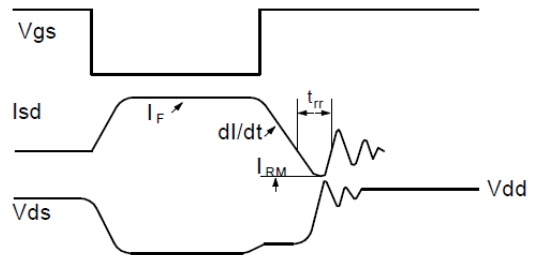
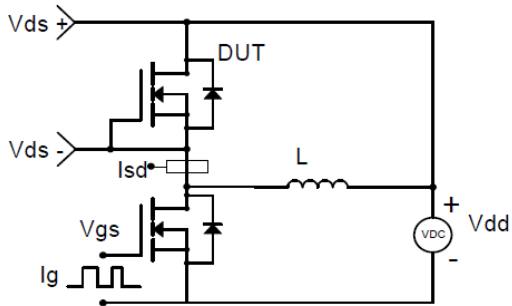


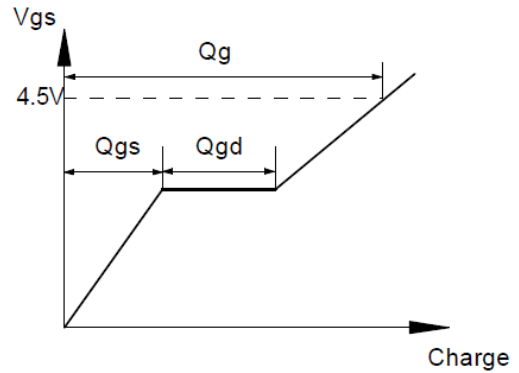
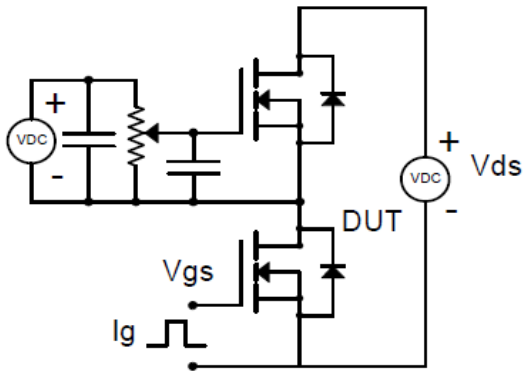
Figure 11. Normalized Maximum Transient Thermal Impedance



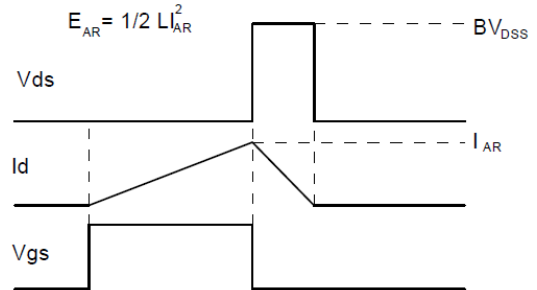
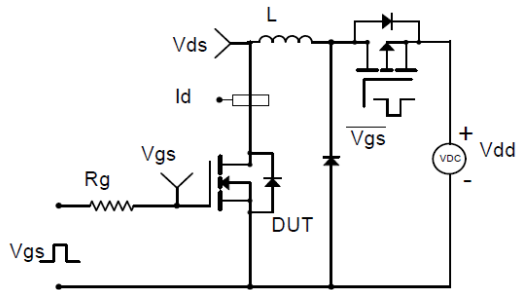
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Gate Charge Test Circuit & Waveform

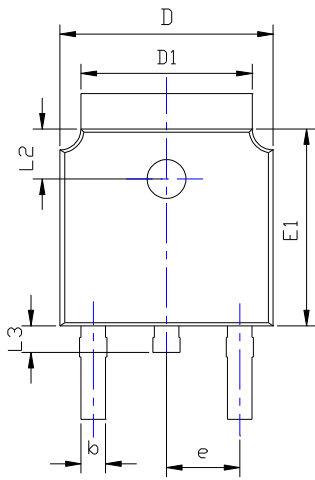


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

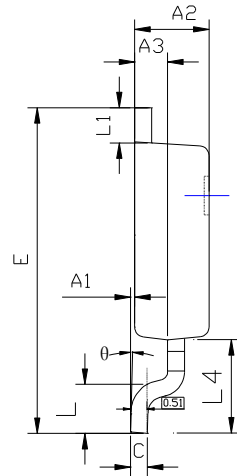


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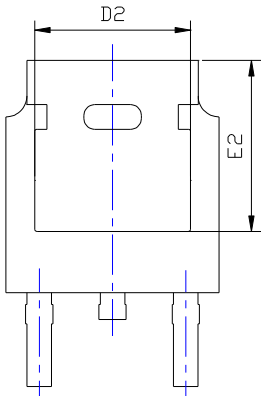
TO-252-B Package information



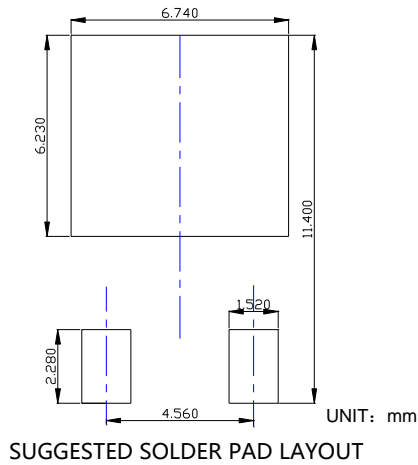
TOP VIEW



SIDE VIEW



BOTTOM VIEW



SYMBOL	DIMENSIONS					
	INCHES			Millimeter		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A1	0.000	---	0.008	0.000	---	0.200
A2	0.087	0.091	0.094	2.200	2.300	2.400
A3	0.035	0.039	0.043	0.900	1.000	1.100
b	0.026	0.030	0.034	0.660	0.760	0.860
c	0.018	0.020	0.023	0.460	0.520	0.580
D	0.256	0.260	0.264	6.500	6.600	6.700
D1	0.203	0.209	0.215	5.150	5.300	5.450
D2	0.181	0.189	0.195	4.600	4.800	4.950
E	0.390	0.398	0.406	9.900	10.100	10.300
E1	0.236	0.240	0.244	6.000	6.100	6.200
E2	0.203	0.209	0.215	5.150	5.300	5.450
e	0.090BSC			2.286BSC		
L	0.049	0.059	0.069	1.250	1.500	1.750
L1	0.035	---	0.050	0.900	---	1.270
L2	0.055	---	0.075	1.400	---	1.900
L3	0.240	0.310	0.039	0.600	0.800	1.000
L4	0.114REF			2.900REF		
θ	0°	---	10°	0°	---	10°

NOTE:

- 1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
- 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
- 3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



YJD80N03B

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