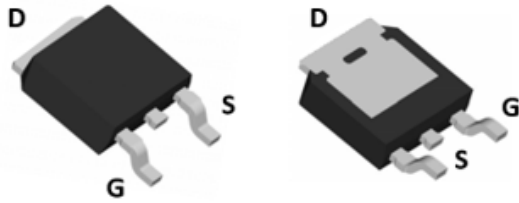
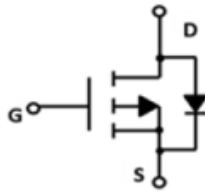


P-Channel Enhancement Mode Field Effect Transistor



TO-252



Product Summary

- V_{DS} -30V
- I_D -70A
- $R_{DS(ON)}$ (at $V_{GS}=-10V$) <6.0mohm
- $R_{DS(ON)}$ (at $V_{GS}=-4.5V$) <10mohm
- 100% UIS Tested
- 100% ∇V_{DS} Tested

General Description

- Trench Power LV MOSFET technology
- High density cell design for Low $R_{DS(ON)}$
- High Speed switching

Applications

- Battery management
- Load switch
- Power management

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	-30	V
Gate-source Voltage		V_{GS}	± 25	V
Drain Current	$T_C=25^\circ\text{C}$	I_D	-70	A
	$T_C=100^\circ\text{C}$		-44	
Pulsed Drain Current ^A		I_{DM}	-200	A
Total Power Dissipation	$T_C=25^\circ\text{C}$	P_D	110	W
	$T_C=100^\circ\text{C}$		44	
Total Power Dissipation	$T_A=25^\circ\text{C}$	P_D	2.5	W
Single Pulse Avalanche Energy ^B		E_{AS}	240	mJ
Thermal Resistance Junction-to-Case ^C		$R_{\theta JC}$	1.14	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction-to-Ambient ^C		$R_{\theta JA}$	50	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ\text{C}$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJD70P03A	F2	YJD70P03A	2500	/	25000	13" reel



YJD70P03A

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =-250μA	-30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-30V, V _{GS} =0V	T _J =25°C		-1	μA
			T _J =55°C		-5	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±25V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =-250μA	-1.2	-1.8	-2.8	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = -10V, I _D =-20A		4.5	6	mΩ
		V _{GS} = -4.5V, I _D =-18A		6.6	10	
Diode Forward Voltage	V _{SD}	I _S =-20A, V _{GS} =0V			-1.2	V
Maximum Body-Diode Continuous Current	I _S				-70	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =-15V, V _{GS} =0V, f=1MHZ		6464		pF
Output Capacitance	C _{oss}			779		
Reverse Transfer Capacitance	C _{rss}			477		
Gate Resistance	R _g	Drain open, f=1Mhz		5.8		Ω
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =-10V, V _{DS} =-15V, I _D =-20A		111.7		nC
Gate-Source Charge	Q _{gs}			21.1		
Gate-Drain Charge	Q _{gd}			22.9		
Reverse Recovery Charge	Q _{rr}	I _F =-15A, di/dt=-100A/us		8.5		
Reverse Recovery Time	t _{rr}			24		
Turn-on Delay Time	t _{D(on)}	V _{GS} = -10V, V _{DD} = -15V, R _G =3Ω, R _L = 0.75Ω		15		ns
Turn-on Rise Time	t _r			75		
Turn-off Delay Time	t _{D(off)}			130		
Turn-off fall Time	t _f			80		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. T_J=25°C, V_{DD}=-20V, V_G=-10V, L=0.5mH.

C. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design, while R_{θJA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



Typical Performance Characteristics

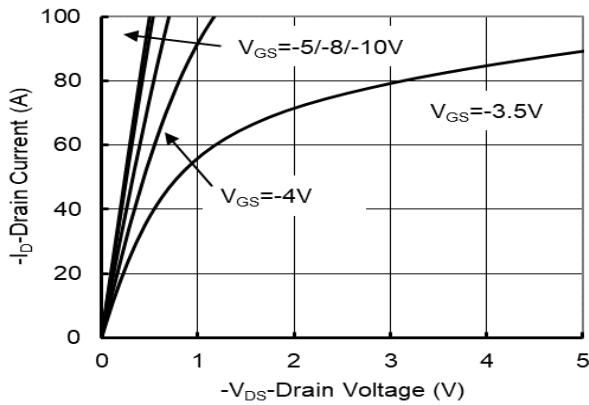


Figure1. Output Characteristics

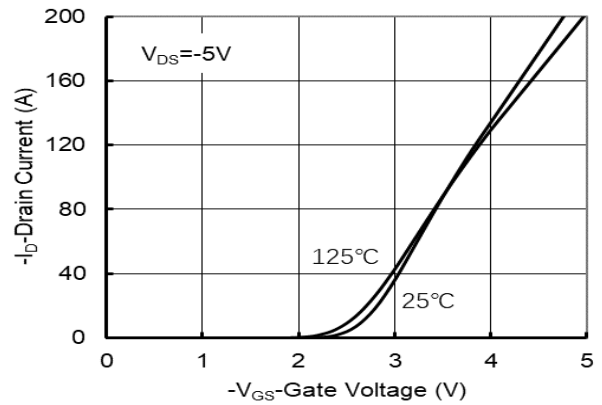


Figure2. Transfer Characteristics

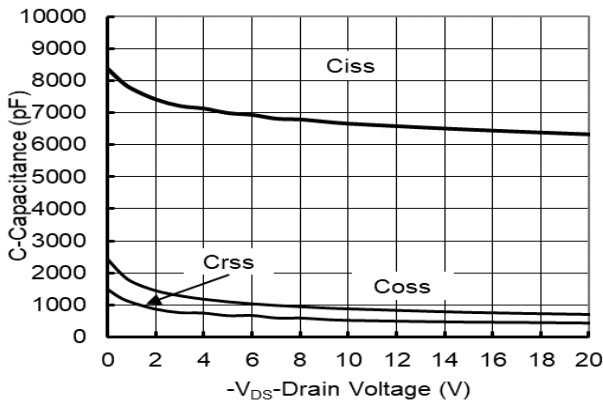


Figure3. Capacitance Characteristics

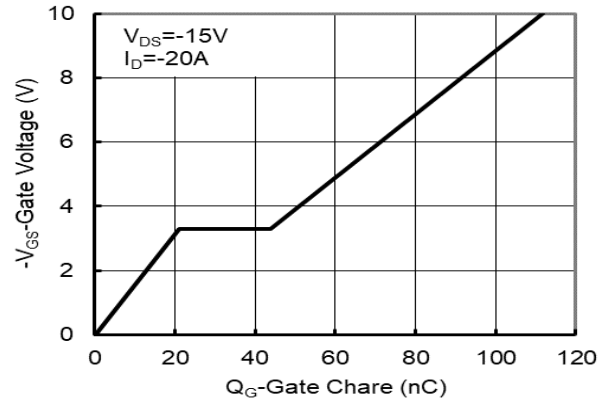


Figure4. Gate Charge

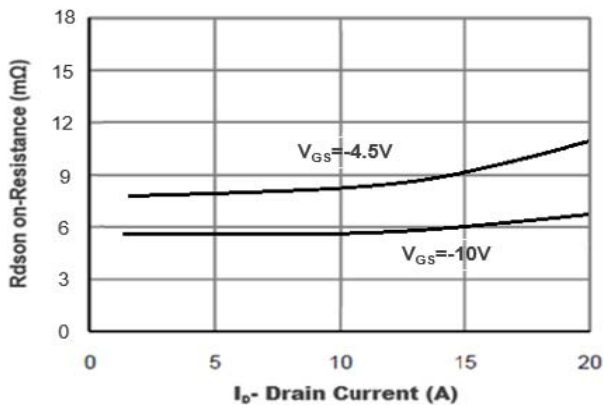


Figure5. Drain-Source on Resistance

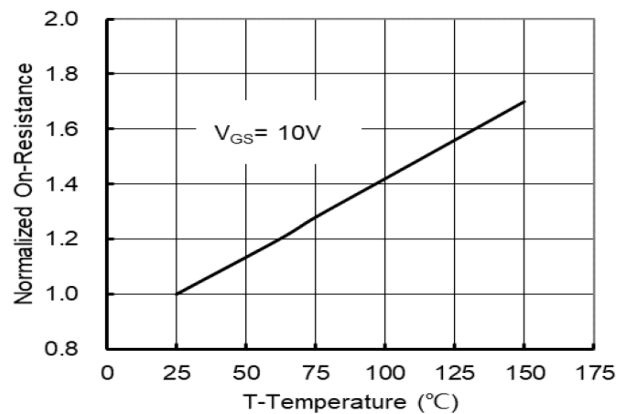


Figure6. Drain-Source on Resistance



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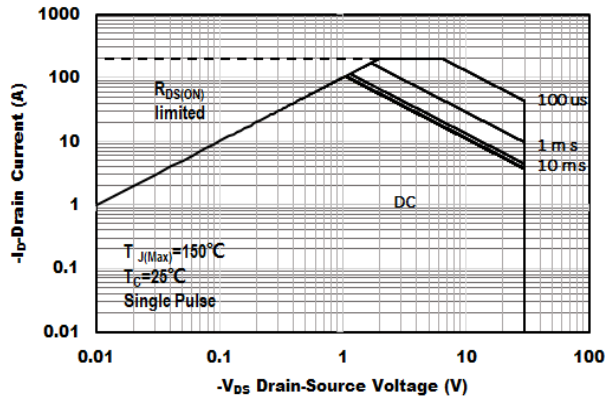


Figure7. Safe Operation Area

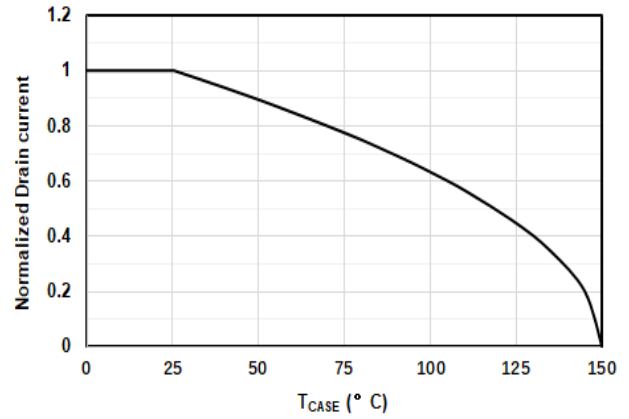


Figure8. Drain current vs. Case Temperature

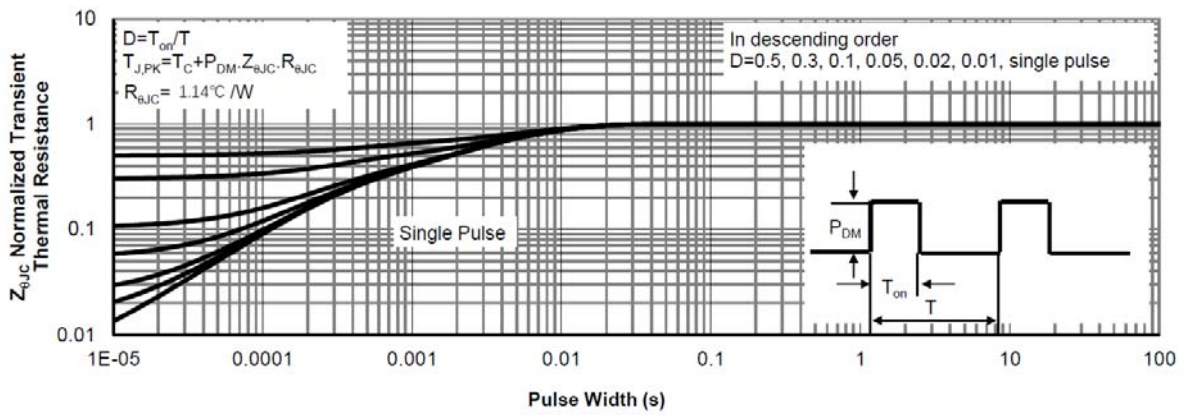
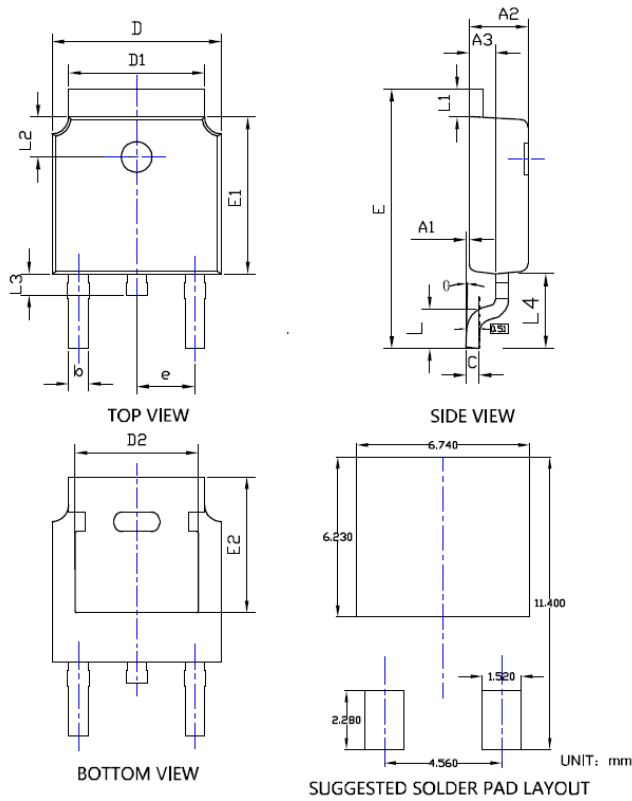


Figure9. Normalized Maximum Transient Thermal Impedance



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■ TO-252 Package information



SYMBOL	DIMENSIONS					
	INCHES			Millimeter		
	MIN.	NDM.	MAX.	MIN.	NDM.	MAX.
A1	0.000	---	0.008	0.000	---	0.200
A2	0.087	0.091	0.094	2.200	2.300	2.400
A3	0.035	0.039	0.043	0.900	1.000	1.100
b	0.026	0.030	0.034	0.660	0.760	0.860
c	0.018	0.020	0.023	0.460	0.520	0.580
D	0.256	0.260	0.264	6.500	6.600	6.700
D1	0.203	0.209	0.215	5.150	5.300	5.450
D2	0.181	0.189	0.195	4.600	4.800	4.950
E	0.390	0.398	0.406	9.900	10.100	10.300
E1	0.236	0.240	0.244	6.000	6.100	6.200
E2	0.203	0.209	0.215	5.150	5.300	5.450
e	0.090BSC			2.286BSC		
L	0.049	0.059	0.069	1.250	1.500	1.750
L1	0.035	---	0.050	0.900	---	1.270
L2	0.055	---	0.075	1.400	---	1.900
L3	0.240	0.310	0.039	0.600	0.800	1.000
L4	0.114REF			2.900REF		
Ø	0*	---	10*	0*	---	10*

NOTE:
 1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
 2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
 3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



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REV.	EFFECTIVE DATE	REVISION HISTORY	PREPARED
1.0	2020.10.20	New release	YanQiang He
1.1	2021.04.27	Change Ciss/Coss/Crss type value from 2504/323/283 to 6464/779/477; Cap, Gate charge and curve updated	YanQiang He