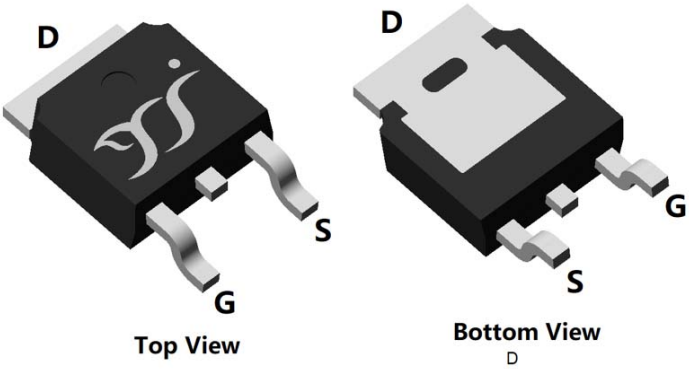
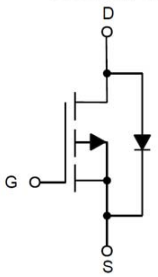
P-Channel Enhancement Mode Field Effect Transistor



TO-252



Product Summary

- V_{DS} -30V
- I_D -45A
- $R_{DS(ON)}$(at V_{GS}=-20V) ＜7.0mohm
- $R_{DS(ON)}$(at V_{GS}=-10V) ＜8.0mohm
- $R_{DS(ON)}$(at V_{GS}=-4.5V) ＜13.0mohm
- 100% EAS Tested
- 100% ▽VDS Tested

General Description

- Trench Power LV MOSFET technology
- High density cell design for Low $R_{DS(ON)}$
- High Speed switching
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Battery protection
- Load switch
- Power management

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	-30	V
Gate-source Voltage		V_{GS}	±25	V
Drain Current	T_C=25℃	I_D	-45	A
	T_C=100℃		-28	
Pulsed Drain Current [A]		I_{DM}	-175	A
Total Power Dissipation	T_C=25℃	P_D	52	W
	T_C=100℃		21	W
Single Pulse Avalanche Energy [B]		E_{AS}	256	mJ
Thermal Resistance Junction-to-Case [C]		$R_{\theta JC}$	2.4	℃/ W
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJD45P03A	F1/F2	YJD45P03A	2500	/	25000	13“ reel

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Static Parameter							
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=-250μA		-30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-30V,V_{GS}=0V	T_J=25℃			-1	μA
			T_J=150℃			-100	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±25V, V_{DS}=0V				±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250μA		-1.2	-1.8	-2.8	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= -20V, I_D=-20A			4.8	7	mΩ
		V_{GS}= -10V, I_D=-15A			5.5	8	
		V_{GS}= -6.0V, I_D=-12A			6.5	12	
		V_{GS}= -4.5V, I_D=-12A			8	13	
Diode Forward Voltage	V_{SD}	I_S=-20A,V_{GS}=0V				-1.2	V
Maximum Body-Diode Continuous Current	I_S					-45	A
Dynamic Parameters							
Input Capacitance	C_{iss}	V_{DS}=-15V,V_{GS}=0V,f=1MHZ			2152		pF
Output Capacitance	C_{oss}				308		
Reverse Transfer Capacitance	C_{rss}				242		
Switching Parameters							
Total Gate Charge	Q_g	V_{GS}=-10V,V_{DS}=-15V,I_D=-12A			40		nC
Gate-Source Charge	Q_{gs}				8.4		
Gate-Drain Charge	Q_{gd}				8.6		
Reverse Recovery Charge	Q_{rr}	I_F=-20A, di/dt=-100A/us			7.8		
Reverse Recovery Time	t_{rr}				18		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-10V,V_{DD}=-15V, I_D=-1A, R_{GEN}=2.5Ω			8		
Turn-on Rise Time	t_r				19		
Turn-off Delay Time	$t_{D(off)}$				75		
Turn-off fall Time	t_f				46		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

B. T_j=25℃, V_{DD}=-25V, V_G=-10V, L=0.5mH, IAS=-32A

C. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ Typical Performance Characteristics

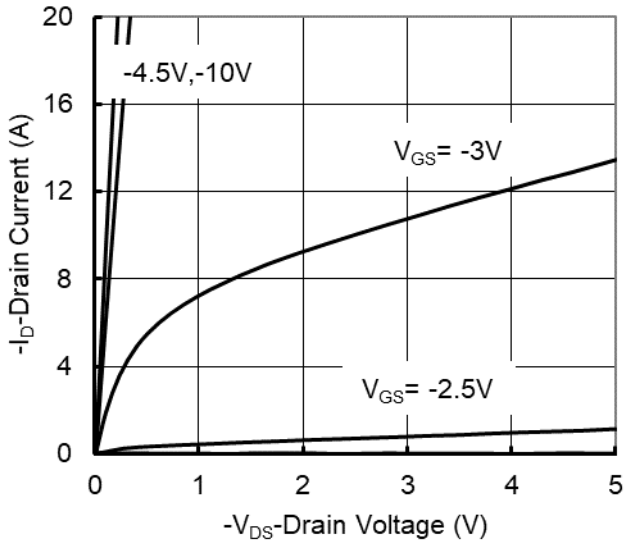


Figure 1. Output Characteristics

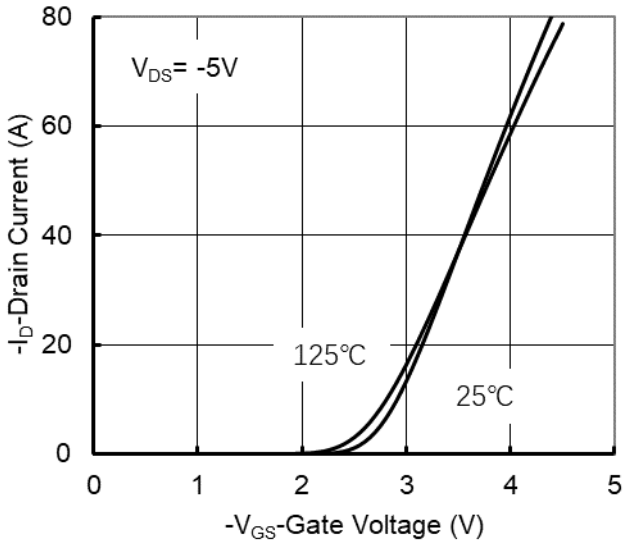


Figure 2. Transfer Characteristics

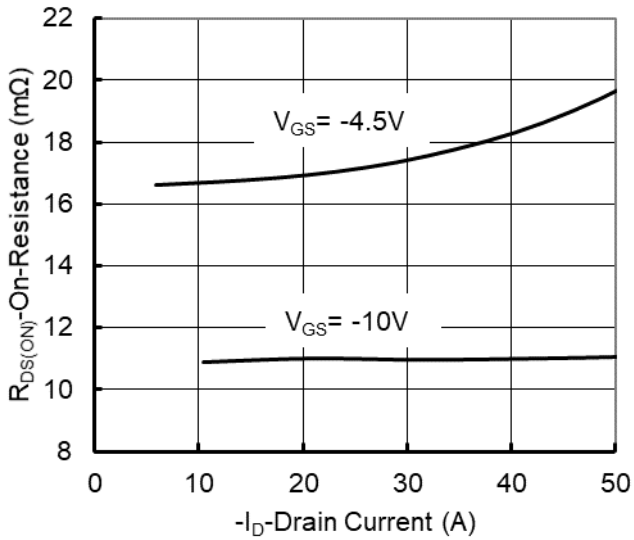


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

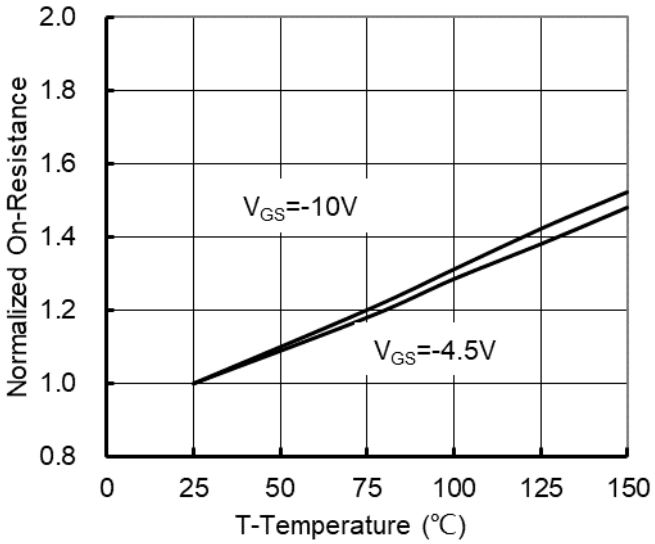


Figure 4. On-Resistance vs. Junction Temperature

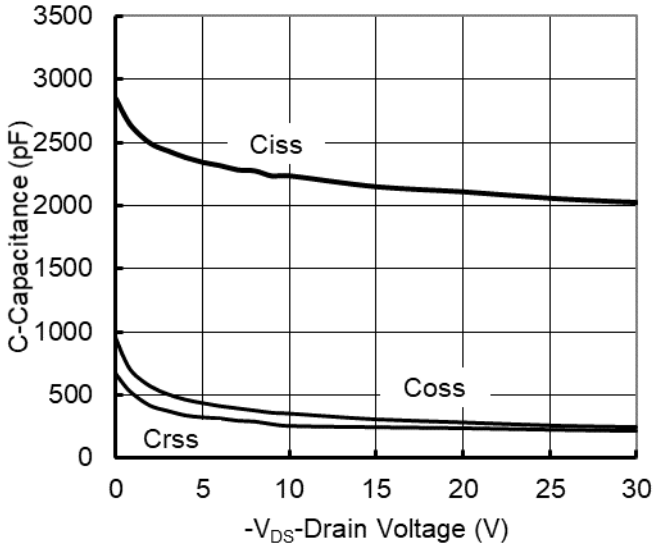


Figure 5. Capacitance Characteristics

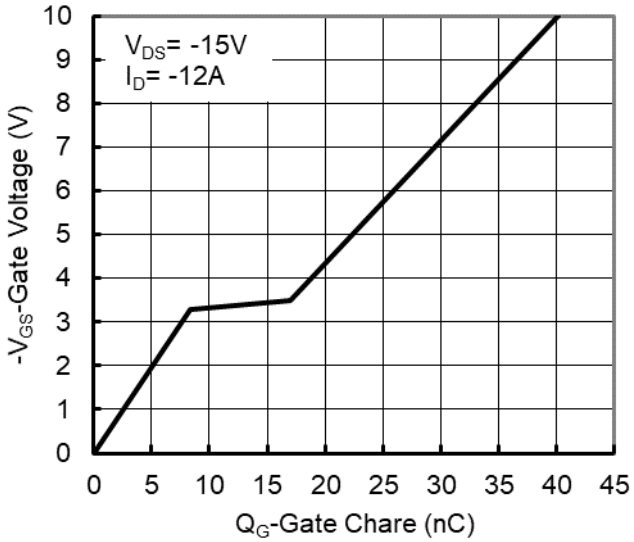


Figure 6. Gate Charge

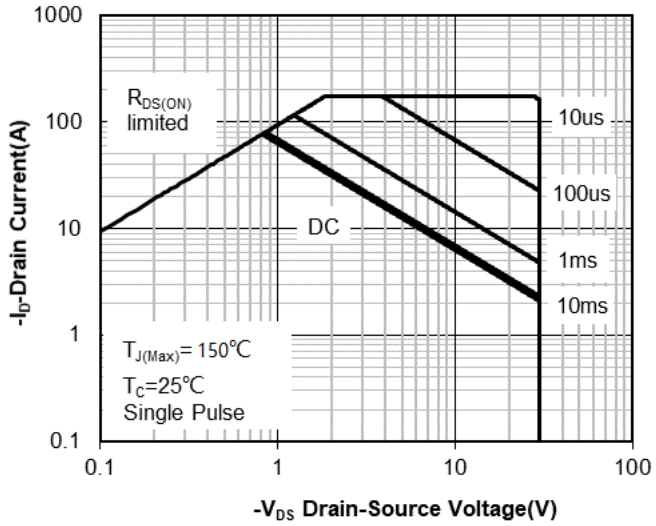


Figure 7. Safe Operation Area

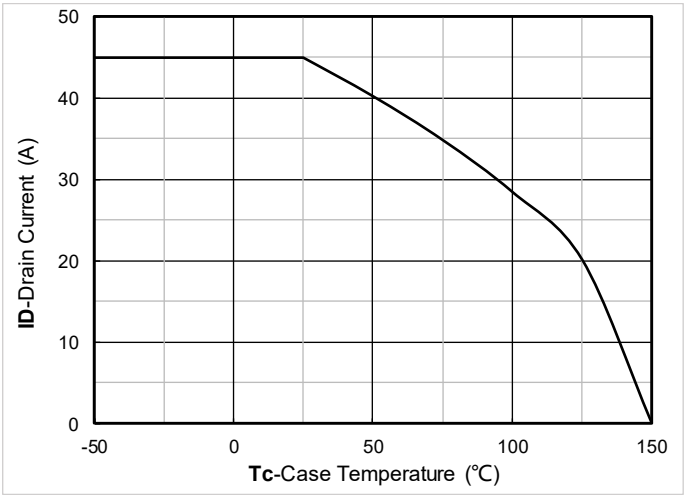


Figure 8. Maximum Continuous Drain Current vs Case Temperature

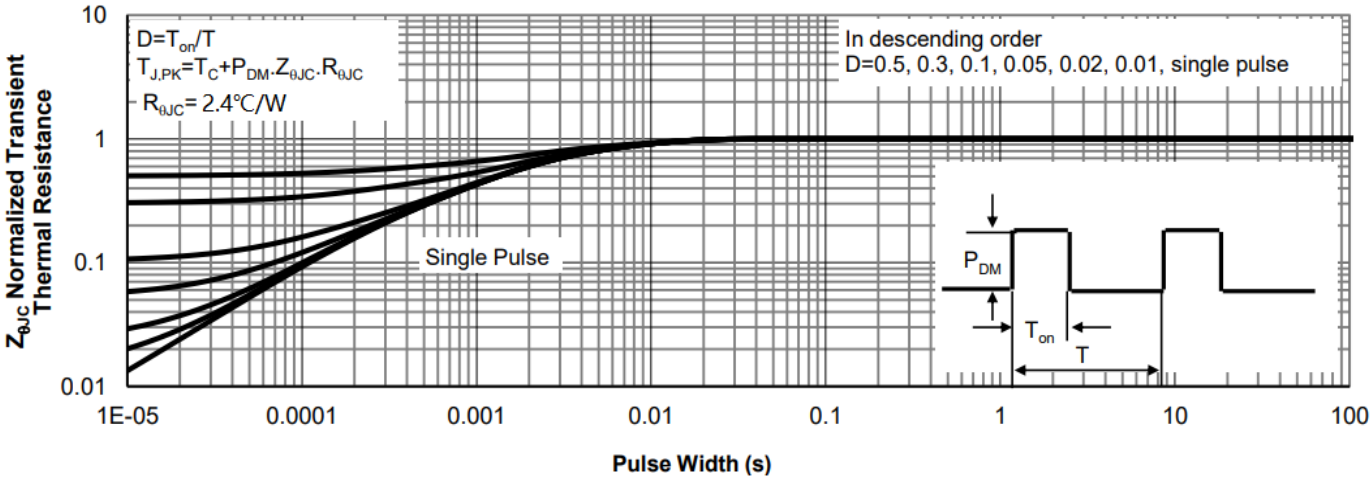
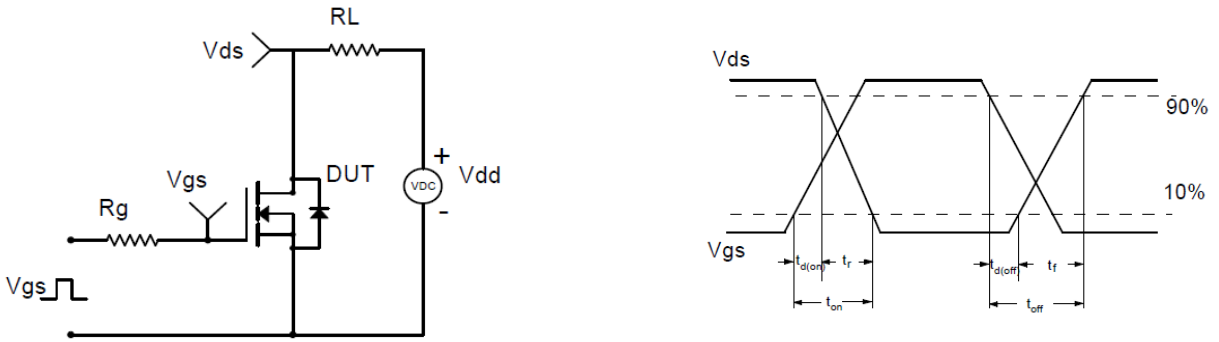
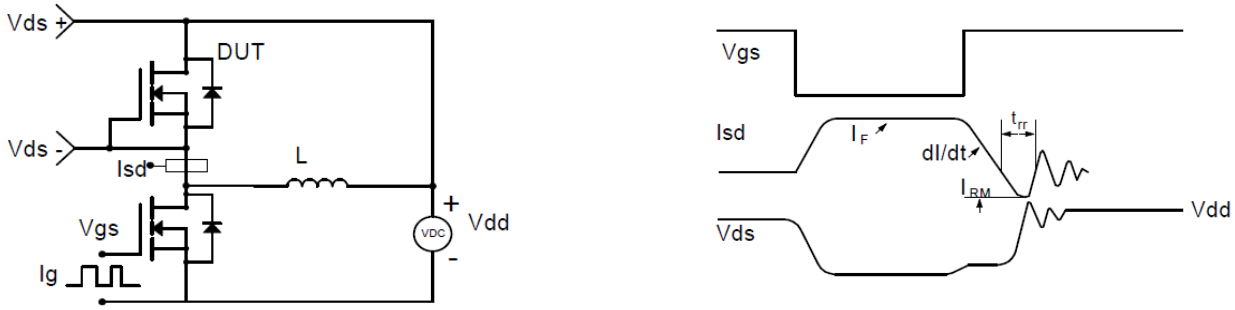


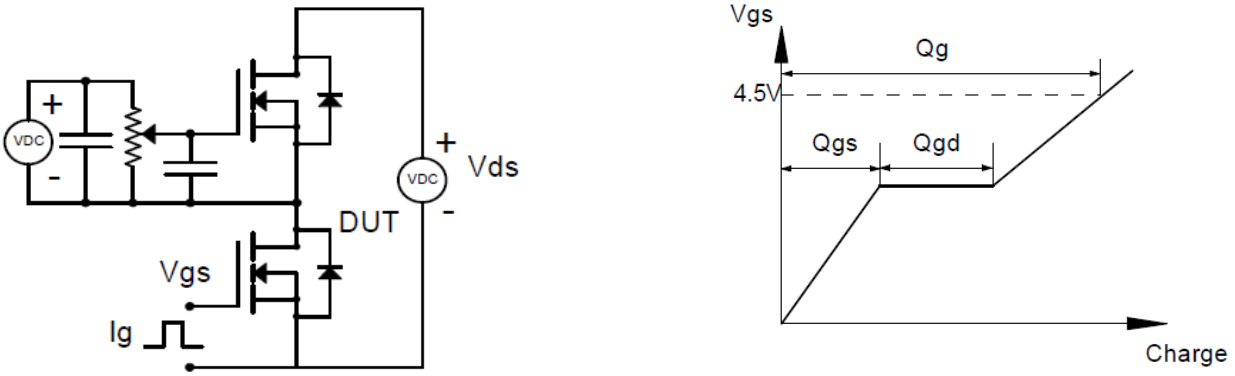
Figure 9. Normalized Maximum Transient Thermal Impedance



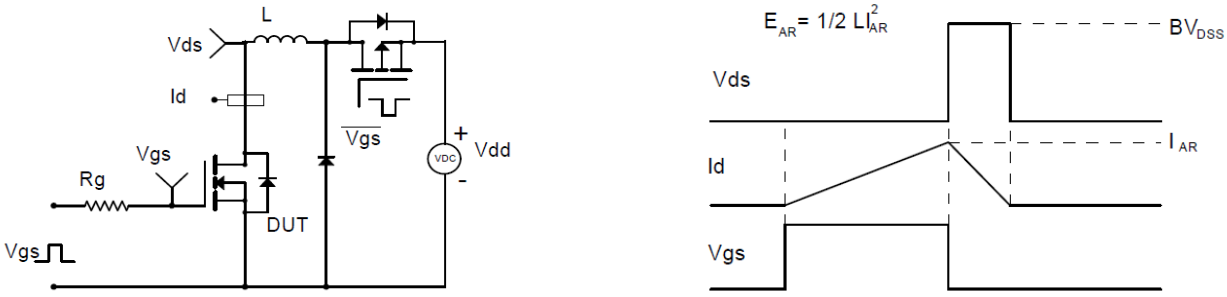
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

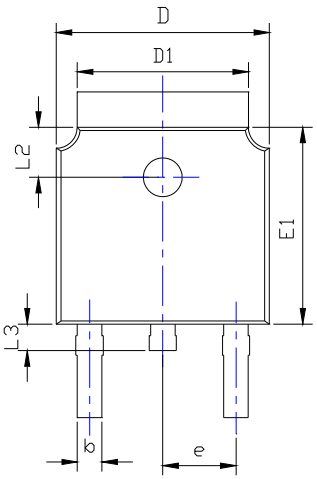


Gate Charge Test Circuit & Waveform

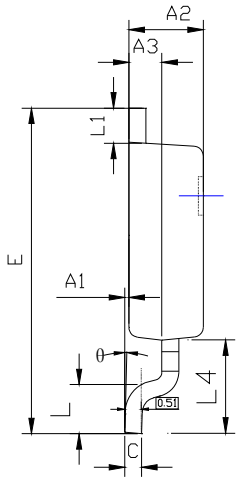


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

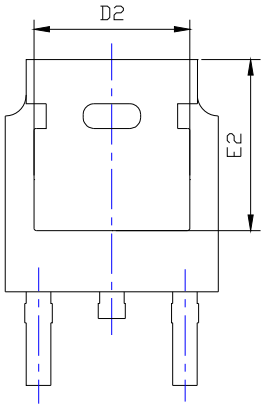
■ TO-252-B Package information



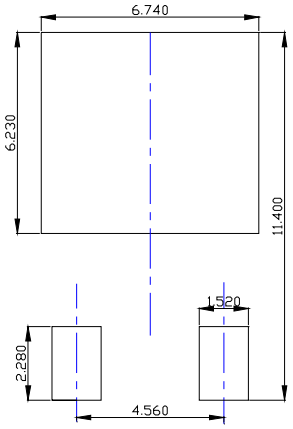
TOP VIEW



SIDE VIEW



BOTTOM VIEW



UNIT：mm

SUGGESTED SOLDER PAD LAYOUT

SYMBOL	DIMENSIONS					
	INCHES			Millimeter		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A1	0.000	---	0.008	0.000	---	0.200
A2	0.087	0.091	0.094	2.200	2.300	2.400
A3	0.035	0.039	0.043	0.900	1.000	1.100
b	0.026	0.030	0.034	0.660	0.760	0.860
c	0.018	0.020	0.023	0.460	0.520	0.580
D	0.256	0.260	0.264	6.500	6.600	6.700
D1	0.203	0.209	0.215	5.150	5.300	5.450
D2	0.181	0.189	0.195	4.600	4.800	4.950
E	0.390	0.398	0.406	9.900	10.100	10.300
E1	0.236	0.240	0.244	6.000	6.100	6.200
E2	0.203	0.209	0.215	5.150	5.300	5.450
e	0.090BSC			2.286BSC		
L	0.049	0.059	0.069	1.250	1.500	1.750
L1	0.035	---	0.050	0.900	---	1.270
L2	0.055	---	0.075	1.400	---	1.900
L3	0.240	0.310	0.039	0.600	0.800	1.000
L4	0.114REF			2.900REF		
θ	0°	---	10°	0°	---	10°

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

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